Contents

BATTERY PROTECTION IC (FOR A 2-SERIAL-CELL PACK) **S-8232 SERIES**

The 8232 is a series of lithium-ion rechargeable battery protection ICs incorporating high-accuracy voltage detection circuits and delay circuits. It is suitable for a 2-serial-cell lithium-ion battery pack.

■ Features

(1) Internal high-accuracy voltage detection circuit

- Over charge detection voltage 3.90 V ± 25 mV to 4.60 V ± 25 mV
  5 mV- step
- Over charge release voltage 3.60 V ± 50 mV to 4.60 V ± 50 mV
  5 mV- step

(The Over charge release voltage can be selected within the range where a difference from Over charge detection voltage is 0 to 0.3 V)

- Over discharge detection voltage 1.70 V ± 80 mV to 2.60 V ± 80 mV
  50 mV- step
- Over discharge release voltage 1.70 V ± 100 mV to 3.80 V ± 100 mV
  50 mV - step

(The Over discharge release voltage can be selected within the range where a difference from Over discharge detection voltage is 0 to 1.2V)

- Over current detection voltage 1 0.07 V ± 20 mV to 0.30 V ± 20 mV
  5 mV-step

(2) High input-voltage device (absolute maximum rating: 18 V)

(3) Wide operating voltage range: 2.0 V to 16 V

(4) The delay time for every detection can be set via an external capacitor.
Each delay time for Over charge detection, Over discharge detection, Over current detection are "Proportion of hundred to ten to one."

(5) Two over current detection levels (protection for short-circuiting)

(6) Internal auxiliary over voltage detection circuit (Fail safe for over voltage)

(7) Internal charge circuit for 0V battery (Unavailable is option)

(8) Low current consumption

- Operation 7.5 μA typ. 14.2 μA max (-40 to +85 °C)
- Power-down mode 0.2 nA typ. 0.1 μA max (-40 to +85 °C)

(9) TSSOP package (8-pin) 6.4 mm×3.1 mm

■ Applications

Lithium-ion rechargeable battery packs

■ Selection Guide(12 Jan , 1998)

Table1

Model/Item	Over charge detection voltage1,2 (VCU1,2)	Over charge release voltage1,2 (VCD1,2)	Over discharge detection voltage1,2 (VDD1,2)	Over discharge release voltage1,2 (VDU1,2)	Over current detection voltage1 (VIOV1)	Over charge detection delay time (tCU) C3=0.22µF	0V battery charging function
S-8232AAFT	4.25V±25mV	4.05±50mV	2.40V±80mV	3.00V±100mV	0.150V±20mV	1.0 sec	Available
S-8232ABFT	4.35V±25mV	4.15±50mV	2.30V±80mV	3.00V±100mV	0.300V±20mV	1.0 sec	Available
S-8232ACFT	4.35V±25mV	4.15±50mV	2.30V±80mV	3.00V±100mV	0.300V±20mV	1.0 sec	Unavailable
S-8232AEFT	4.35V±25mV	4.28±50mV	2.15V±80mV	2.80V±100mV	0.100V±20mV	1.0 sec	Available
S-8232AFFT	4.25V±25mV	4.05±50mV	2.30V±80mV	2.70V±100mV	0.300V±20mV	1.0 sec	Available
S-8232AGFT	4.25V±25mV	4.05±50mV	2.20V±80mV	2.40V±100mV	0.200V±20mV	1.0 sec	Available
S-8232AHFT	4.25V±25mV	4.05±50mV	2.20V±80mV	2.40V±100mV	0.300V±20mV	1.0 sec	Available
S-8232AIFT	4.325V±25mV	4.325V *1,2	2.40V±80mV	3.00V±100mV	0.300V±20mV	1.0 sec	Unavailable
S-8232AJFT	4.25V±25mV	4.05±50mV	2.40V±80mV	3.00V±100mV	0.150V±20mV	1.0 sec	Unavailable
S-8232AKFT	4.20V±25mV	4.00±50mV	2.30V±80mV	2.90V±100mV	0.200V±20mV	1.0 sec	Available
S-8232ALFT	4.30V±25mV	4.05±50mV	2.00V±80mV	3.00V±100mV	0.200V±20mV	1.0 sec	Available

*1) Without over charge detection hysteresis.

*2) Auxiliary over charge detection voltage1,2(VCUaux1,2) is VCUaux1,2=1.11×VCU1,2(Over charge detection voltage1,2) which is fixed internally. The others are VCUaux1,2 = 1.25×VCU1,2

Change in the detection voltage is available in products other than the above listed ones.
Please contact with our sales division.

The over discharge detection voltage can be selected within the range from 1.7 to 3.0V.
When the Over discharge detection voltage is higher than 2.6V, the Over charge detection voltage and the Over charge release voltage are limited as table 2.

Table 2

Over discharge detection voltage1,2 (VDD1,2)	Over charge detection voltage1,2 (VCU1,2)	Voltage difference between Over charge detection voltage and Over charge release voltage (VCU1,2 - VCD1,2)
1.70 to 2.60 V	3.90 to 4.60 V	0 to 0.30 V
1.70 to 2.80 V	3.90 to 4.60 V	0 to 0.20 V
1.70 to 3.00 V	3.90 to 4.50 V	0 to 0.10 V

■ Block Diagram

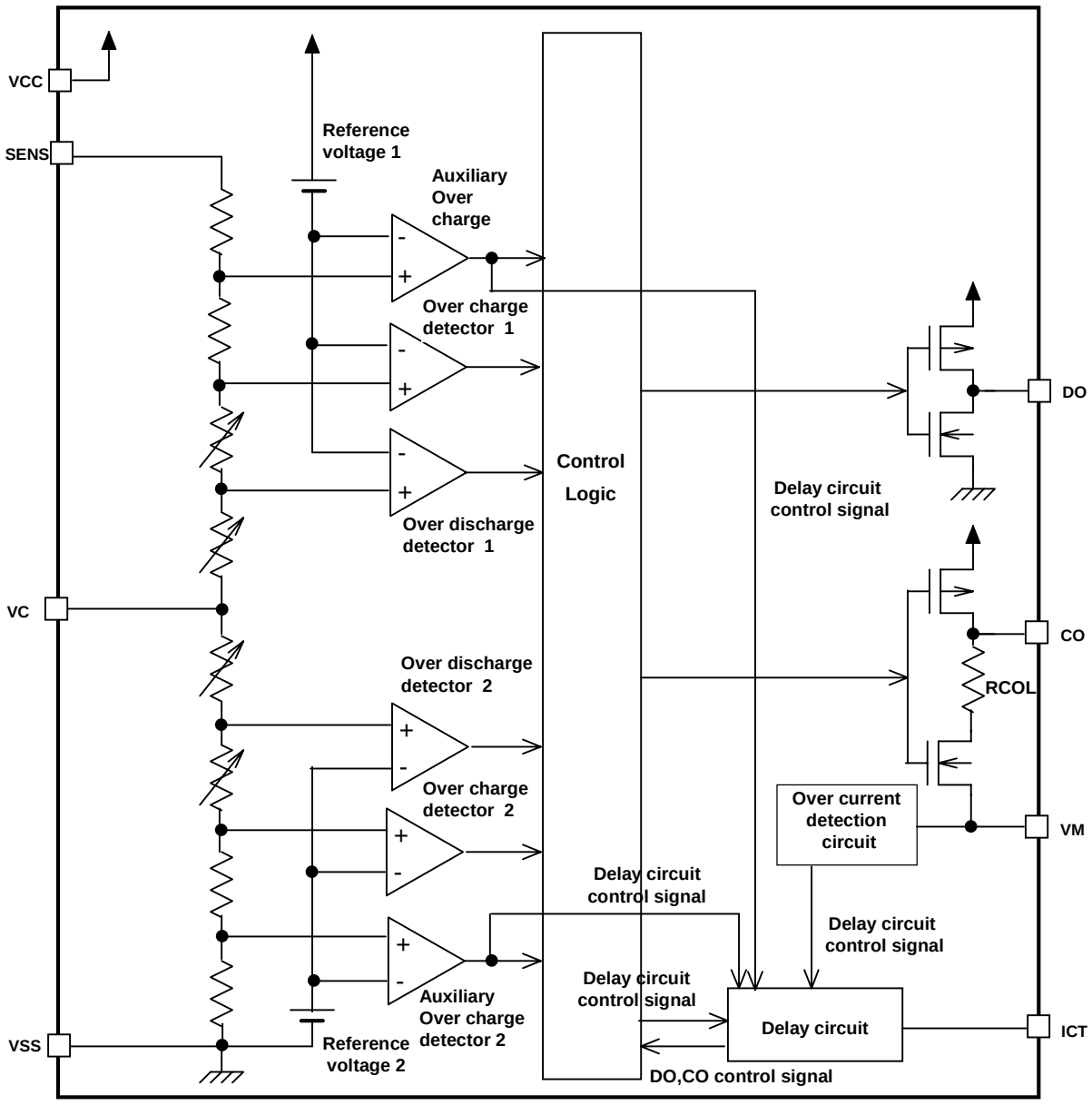
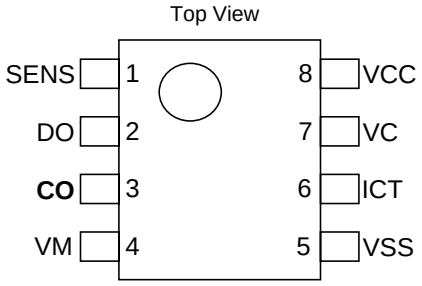


Figure 1

Output impedance when CO terminal output ‘L’ is higher than DO terminal. RCOL resistor is connected with CO terminal. Please refer ‘Electric Characteristics’.

■ Pin Assignment



TSSOP-8

Figure 2

■ Pin Description

Table 3

No.	Name	Description
1	SENS	Detects pin for VCC voltage (Connects battery1 positive voltage)
2	DO	Connects FET gate for discharge control (CMOS output)
3	CO	Connects FET gate for charge control (CMOS output)
4	VM	Detects pin for VM voltage (Over current detection pin)
5	VSS	Negative power input pin (Connects battery2 negative voltage)
6	ICT	Connects capacitor for delay circuit
7	VC	The middle pin between two batteries (Connects battery1 negative voltage and battery2 positive voltage)
8	VCC	Positive power input pin (Connects battery1 positive voltage)

■ Absolute Maximum Ratings

Table 4 Ta = 25°C

Item	Symbol	Applied Pins	Rating	Unit
Input voltage between VCC and VSS	VDS	VCC	VSS-0.3 to VCC+18	V
ICT Input terminal voltage	VICT	ICT	VSS-0.3 to VCC+0.3	V
VM Input terminal voltage	VVM	VM	VCC-18 to VCC+0.3	V
DO output terminal voltage	VDO	DO	VSS-0.3 to VCC+0.3	V
CO output terminal voltage	VCO	CO	VVM-0.3 to VCC+0.3	V
Power dissipation	PD		300	mW
Operating temperature range	Topr		-40 to +85	°C
Storage temperature range	Tstg		-40 to +125	°C

■ Electrical Characteristics

Table 5 Ta = 25°C

	Symbol	Condition	Circuit	Notice	Min.	Typ.	Max.	Unit
Detection voltage								
Over charge detection voltage 1,2	VCU1,2	1,2	1	3.90 to 4.60 Adjustment	VCU1,2 -0.025	VCU1,2	VCU1,2 +0.025	V
Auxiliary over charge detection voltage 1,2 VCUaux1,2 = VCU1,2×1.25 or VCUaux1,2 = VCU1,2×1.11	VCUaux1,2	1,2	1	VCU1,2×1.25 Fixed Type	VCU1,2 ×1.21	VCU1,2 ×1.25	VCU1,2 ×1.29	V
	VCUaux1,2	1,2	1	VCU1,2×1.11 Fixed Type	VCU1,2 ×1.07	VCU1,2 ×1.11	VCU1,2 ×1.15	V
Over charge release voltage 1,2	VCD1,2	1,2	1	3.60 to 4.60 Adjustment	VCD1,2 -0.050	VCD1,2	VCD1,2 +0.050	V
Over discharge detection voltage 1,2	VDD1,2	1,2	1	1.70 to 2.60 Adjustment	VDD1,2 -0.080	VDD1,2	VDD1,2 +0.080	V
Over discharge release voltage 1,2	VDU1,2	1,2	1	1.70 to 3.80 Adjustment	VDU1,2 -0.100	VDU1,2	VDU1,2 +0.100	V
Over current detection voltage 1	VIOV1	3	1	0.07 to 0.30 Adjustment	VIOV1-0.020	VIOV1	VIOV1+0.020	V
Over current detection voltage 2	VIOV2	3	1	VCC Reference	-1.57	-1.20	-0.83	V
Voltage temperature factor 1	TCOE1			(*1) Ta=-40 to 85°C	-0.6	0	0.6	mV/°C
Voltage temperature factor 2	TCOE2			(*2) Ta=-40 to 85°C	-0.24	-0.05	0	mV/°C
Delay time(C3=0.22μF)								
Over charge detection delay time1,2	tCU1,2	8,9	5	1.0 S	0.73	1.00	1.35	S
Over discharge detection delay time 1,2	tDD1,2	8,9	5	0.1 S	68	100	138	mS
Over current detection delay time1	tIOV1	10	5	0.01 S	6.7	10	13.9	mS
Input voltage								
Input voltage between VCC and VSS				absolute maximum rating	-0.3	---	18	
Operating voltage								
Operating voltage between VCC and VSS	VDSOP			(*3)	2.0	---	16	V
Current consumption								
Current consumption during normal operation	IOPE	4	2	V1=V2=3.6V	2.1	7.5	12.7	μA
Current consumption at power down	IPDN	4	2	V1=V2=1.5V	0	0.0002	0.04	μA
Output voltage								
DO"H"voltage	VDO(H)	6	3	at Iout=10uA	VCC-0.05	VCC-0.003	---	V
DO"L"voltage	VDO(L)	6	3	at Iout=10uA	---	VSS+0.003	VSS+0.05	V
CO"H"voltage	VCO(H)	7	4	at Iout=10uA	VCC-0.15	VCC-0.019	---	V
CO pin internal resistance								
Resistance between VSS and CO	RCOL	7	4	VSS-CO=4.7V×2	0.29	0.6	1.44	MΩ
Internal resistance								
Resistance between VCC and VM	Rvcm	5	2	Vcc-VM=0.5V	105	240	575	KΩ
Resistance between VSS and VM	Rvsm	5	2	VM-VSS=1.1V	511	597	977	KΩ
0V battery charging function								
0V charge starting voltage	V0CHA	11	6	0V batt. Cha. Available	0.38	0.75	1.12	V
0V charge inhibiting voltage 1,2	V0INH1,2	12,13	6	0V batt. Cha. Unavailable	0.32	0.88	1.44	V

(*1)Voltage temperature factor 1 indicates over charge detection voltage, over charge release voltage, over discharge detection voltage, and over discharge release voltage.

(*2)Voltage temperature factor 2 indicates over current detection voltage.

(*3)The DO and CO logic must be established for the operating voltage.

Table 6 Ta = -40 to +85°C

	Symbol	Condition	Circuit	Notice	Min.	Typ.	Max.	Unit
Detection voltage								
Over charge detection voltage 1,2	VCU1,2	1,2	1	3.90 to 4.60 Adjustment	VCU1,2 -0.055	VCU1,2	VCU1,2 +0.045	V
Auxiliary over charge detection voltage 1,2 VCUaux1,2 = VCU1,2×1.25 or VCUaux1,2 = VCU1,2×1.11	VCUaux1,2	1,2	1	VCU1,2×1.25 Fixed. Type	VCU1,2 ×1.19	VCU1,2 ×1.25	VCU1,2 ×1.31	V
	VCUaux1,2	1,2	1	VCU1,2×1.11 Fixed. Type	VCU1,2 ×1.05	VCU1,2 ×1.11	VCU1,2 ×1.17	V
Over charge release voltage 1,2	VCD1,2	1,2	1	3.60 to 4.60 Adjustment	VCD1,2 -0.080	VCD1,2	VCD1,2 +0.070	V
Over discharge detection voltage 1,2	VDD1,2	1,2	1	1.70 to 2.60 Adjustment	VDD1,2 -0.110	VDD1,2	VDD1,2 +0.100	V
Over discharge release voltage 1,2	VDU1,2	1,2	1	1.70 to 3.80 Adjustment	VDU1,2 -0.130	VDU1,2	VDU1,2 +0.120	V
Over current detection voltage 1	VIOV1	3	1	0.07 to 0.30 Adjustment	VIOV1-0.033	VIOV1	VIOV1+0.033	V
Over current detection voltage 2	VIOV2	3	1	VCC Reference	-1.70	-1.20	-0.71	V
Voltage temperature factor 1	TCOE1			(*1) Ta=-40 to 85°C	-0.6	0	0.6	mV/°C
Voltage temperature factor 2	TCOE2			(*2) Ta=-40 to 85°C	-0.24	-0.05	0	mV/°C
Delay time(C3=0.22µF)								
Over charge detection delay time1,2	tCU1,2	8,9	5	1.0 S	0.55	1.00	2.06	S
Over discharge detection delay time 1,2	tDD1,2	8,9	5	0.1 S	67	100	141	mS
Over current detection delay time1	tIOV1	10	5	0.01 S	6.3	10	14.7	mS
Input voltage								
Input voltage between VCC and VSS				absolute maximum rating	-0.3	---	18	
Operating voltage								
Operating voltage between VCC and VSS	VDSOP			(*3)	2.0	---	16	V
Current consumption								
Current consumption during normal operation	IOPE	4	2	V1=V2=3.6V	1.8	7.5	14.2	µA
Current consumption at power down	IPDN	4	2	V1=V2=1.5V	0	0.0002	0.10	µA
Output voltage								
DO"H"voltage	VDO(H)	6	3	at Iout=10uA	VCC-0.17	VCC-0.003	---	V
DO"L"voltage	VDO(L)	6	3	at Iout=10uA	---	VSS+0.003	VSS+0.17	V
CO"H"voltage	VCO(H)	7	4	at Iout=10uA	VCC-0.27	VCC-0.019	---	V
CO pin internal resistance								
Resistance between VSS and CO	RCOL	7	4	VSS-CO=4.7V×2	0.22	0.6	2.20	MΩ
Internal resistance								
Resistance between VCC and VM	Rvcm	5	2	Vcc-VM=0.5V	79	240	878	KΩ
Resistance between VSS and VM	Rvsm	5	2	VM-VSS=1.1V	387	597	1491	KΩ
0V battery charging function								
0V charge starting voltage	V0CHA	11	6	0V batt. Cha. Available	0.26	0.75	1.25	V
0V charge inhibiting voltage 1,2	V0INH1,2	12,13	6	0V batt. Cha. Unavailable	0.20	0.88	1.57	V

(*1)Voltage temperature factor 1 indicates over charge detection voltage, over charge release voltage, over discharge detection voltage, and over discharge release voltage.

(*2)Voltage temperature factor 2 indicates over current detection voltage.

(*3)The DO and CO logic must be established for the operating voltage.

■ Measurement Circuits

(1) Measurement 1 Measurement circuit 1

Set S1=OFF, V1=V2=3.6 V, and V3=0V under normal condition. Increase V1 from 3.6 V gradually.
The V1 voltage when CO = 'L' is over charge detection voltage 1 (VCU1). Decrease V1 gradually.
The V1 voltage when CO = 'H' is over charge release voltage 1 (VCD1). Further decrease V1.
The V1 voltage when DO = 'L' is over discharge voltage 1 (VDD1). Increase V1 gradually.
The V1 voltage when DO = 'H' is over discharge release voltage 1 (VDU1).
Set S1=ON,and V1=V2=3.6 V and V3=0V under normal condition. Increase V1 from 3.6 V gradually.
The V1 voltage when CO = 'L' is auxiliary over charge detection voltage 1 (VCUaux1).

(2) Measurement 2 Measurement circuit 1

Set S1=OFF,V1=V2=3.6 V ,and V3=0V under normal condition. Increase V2 from 3.6 V gradually.
The V2 voltage when CO = 'L' is over charge detection voltage 2 (VCU2). Decrease V2 gradually.
The V2 voltage when CO = 'H' is over charge release voltage 2 (VCD2). Further decrease V2.
The V2 voltage when DO = 'L' is over discharge voltage 2 (VDD2). Increase V2 gradually.
The V2 voltage when DO = 'H' is over discharge release voltage 2 (VDU2).
Set S1=ON,and V1=V2=3.6 V and V3=0V under normal condition. Increase V2 from 3.6 V gradually.
The V2 voltage when CO = 'L' is auxiliary over charge detection voltage 2 (VCUaux2).

(3) Measurement 3 Measurement circuit 1

Set S1=OFF,V1=V2=3.6 V , and V3=0V under normal condition. Increase V3 from 0V gradually.
The V3 voltage when DO = 'L' is over current detection voltage 1 (VIOV1).
Set S1=ON,V1=V2=3.6 V,V3=0 under normal condition. Increase V3 from 0V gradually.(The voltage change rate < 1.0V/msec) (V1+V2-V3) voltage when DO = 'L' is over current detection voltage 2 (VIOV2).

(4) Measurement 4 Measurement circuit 2

Set S1=ON, V1=V2=3.6 V, and V3=0 V under normal condition and measure current consumption.
Current consumption I1 is the normal condition current consumption (IOPE).
Set S1=OFF, V1=V2=1.5 V under over discharge condition and measure current consumption.
Current consumption I1 is the power-down current consumption (IPDN).

(5) Measurement 5 Measurement circuit 2

Set S1=ON, V1=V2=V3=1.5 V, and V3=2.5V under over discharge condition. (V1+V2-V3)/I2 is the internal resistance between VCC and VM (Rvcm).
Set S1=ON, V1=V2=3.5V, and V3=1.1 V under over current condition. V3/I2 is the internal resistance between VSS and VM (Rvsm).

(6) Measurement 6 Measurement circuit 3

Set S1=ON, S2=OFF, V1=V2=3.6 V, and V3=0V under normal condition. Increase V4 from 0 V gradually. The V4 voltage when I1 = 10 μA is DO'H' voltage (VD0 (H)).
Set S1=OFF, S2=ON, V1=V2=3.6 V, and V3=0.5 V under over current condition. Increase V5 from 0 V gradually. The V5 voltage when I2 = 10 μA is the DO'L' voltage (VDO (L)).

(7) Measurement 7 Measurement circuit 4

Set S1=ON, S2=OFF, V1=V2=3.6 V and V3=0 V under normal condition. Increase V4 from 0 V gradually. The V4 voltage when I1 = 10 μA is the CO'H' voltage (VC0 (H)).
Set S1=OFF S2=ON, V1=V2=4.7, V3=0V, and V4=9.4V under over voltage condition. (V5)/I2 is the CO pin internal resistance (RCOL).

(8) Measurement 8 Measurement circuit 5

Set V1=V2=3.6 V, and V3=0V under normal condition. Increase V1 from (VCU1-0.2V) to (VCU1+0.2V) immediately (within 10 μs). The time after V1 becomes (VCU1+0.2V) until CO goes 'L' is the over charge detection delay time 1 (tCU1).
Set V1=V2=3.5 V, and V3=0V under normal condition. Decrease V1 from (VDD1+0.2V) to (VDD1-0.2V) immediately (within 10 μs). The time after V1 becomes (VDD1-0.2V) until DO goes 'L' is the over discharge detection delay time 1 (tDD1).

(9) Measurement 9 Measurement circuit 5

Set V1=V2=3.6 V , and V3=0V under normal condition. Increase V2 from (VCU2-0.2V) to (VCU2+0.2V) immediately (within 10 μs). The time after V2 becomes (VCU2+0.2V) until CO goes 'L' is the over charge detection delay time 2 (tCU2).
Set V1=V2=3.6 V , and V3=0V under normal condition. Decrease V2 from (VDD2+0.2V) to (VDD2-0.2V) immediately (within 10 μs). The time after V2 becomes (VDD2-0.2V) until DO goes 'L' is the over discharge detection delay time 2 (tDD2).

(10) Measurement 10 Measurement circuit 5

Set V1=V2=3.6 V, and V3=0V under normal condition. Increase V3 from 0 V to 0.5 V immediately (within 10 μs). The time after V3 becomes 0.5 V until DO goes 'L' is the over current detection delay time 1 (tI0V1).

(11) Measurement 11 Measurement circuit 6

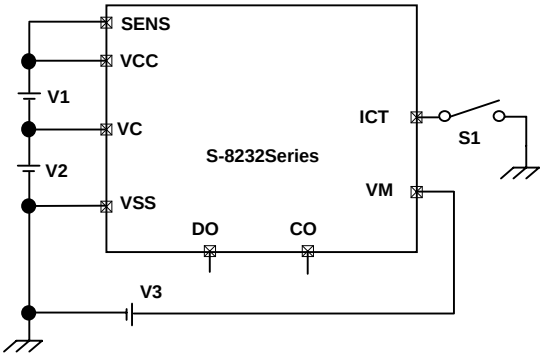
Set V1=V2=0 V, and V3=2 V, and decrease V3 gradually. The V3 voltage when CO = 'L' (VCC- 0.3 V or lower) is the 0V charge starting voltage (V0CHA).

(12) Measurement 12 Measurement circuit 6

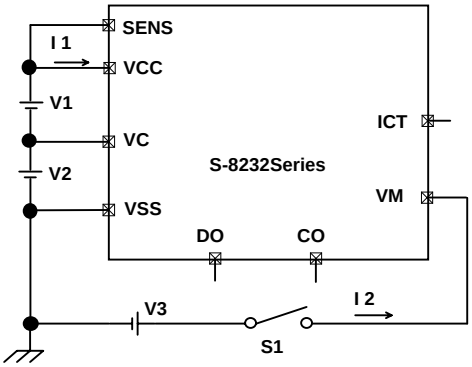
Set V1=0 V, V2=3.6 V, and V3=12 V, and increase V1 gradually. The V1 voltage when CO = 'H' (VM+ 0.3 V or higher) is the 0V charge inhibiting voltage 1 (V0INH1).

(13) Measurement 13 Measurement circuit 6

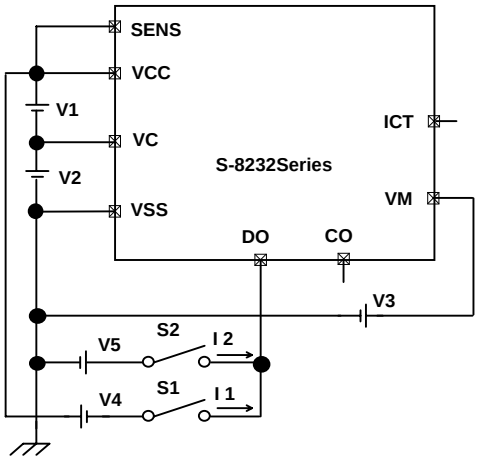
Set V1=3.6 V, V2=0 V, and V3=12 V, and increase V2 gradually. The V2 voltage when CO = 'H' (VM+ 0.3 V or higher) is the 0V charge inhibiting voltage 2 (V0INH2).



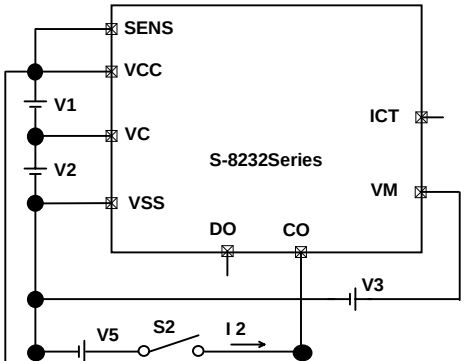
Measurement circuit 1



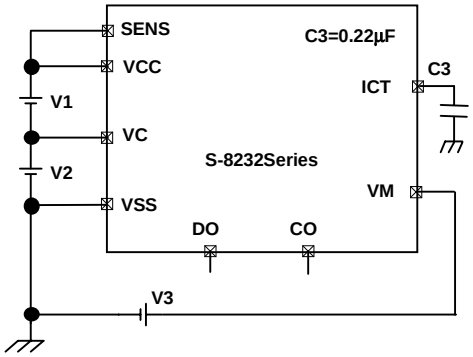
Measurement circuit 2



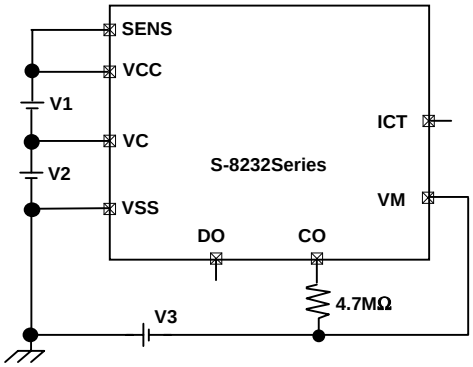
Measurement circuit 3



Measurement circuit 4



Measurement circuit 5



Measurement circuit 6

■ Description

Normal condition(*1)

This IC monitors the voltages of the two serially-connected batteries and the discharge current to control charging and discharging. If the voltages of all the two batteries are in the range from the over discharge detection voltage (VDD1,2) to the over charge detection voltage (VCU1,2), and the current flowing through the batteries becomes equal or lower than a specified value (the VM terminal voltage is equal or lower than over current detection voltage 1), the charging and discharging FET's turn on. In this condition, charging and discharging can be carried out freely. This condition is called the normal condition. In this condition, the VM and VSS terminals are shorted by the Rvsm resistor.

Over current condition

This IC is provided with the two over current detection levels (VIOV1 and VIOV2) and the two over current detection delay time (tIOV1 and tIOV2) corresponding to each over current detection level.

If the discharging current becomes equal to or higher than a specified value (the VM terminal voltage is equal to or higher than the over current detection voltage) during discharging under normal condition and it continues for the over current detection delay time (tIOV) or longer, the discharging FET turns off to stop discharging. This condition is called an over current condition. The VM and VSS terminals are shorted by the Rvsm resistor at this time. The charging FET turns off.
When the discharging FET is off and a load is connected, the VM terminal voltage equals the VCC potential. The over current condition returns to the normal condition when the load is released and the impedance between the EB- and EB+ terminals (see Figure 6 for a connection example) is 200MΩ or higher. When the load is released, the VM terminal, which and the VSS terminal are shorted with the Rvsm resistor, goes back to the VSS potential. The IC detects that the VM terminal potential returns to over current detection voltage 1 (VIOV1) or lower and returns to the normal condition.

Over charge condition

The over charge condition is detected in two cases:

1) If one of the battery voltages becomes higher than the over charge detection voltage (VCU1,2) during charging under normal condition and it continues for the over charge detection delay time (tCU1,2) or longer, the charging FET turns off to stop charging.
2) If one of the battery voltages becomes higher than the auxiliary over charge detection voltage (VCUaux1,2) the charging FET turns off immediately to stop charging.

The VM and VSS terminals are shorted by the Rvsm resistor under the over charge condition.

The auxiliary over charge detection voltage (VCUaux1,2) is fixed internally and calculated by the over charge detection voltage (VCU1,2) as follows:

$$VCUaux1,2\ [V] = 1.25 \times VCU1,2\ [V]$$

[For without Over charge detection / release hysteresis type (VCU1,2 = VCD1,2)]

$$VCUaux1,2\ [V] = 1.11 \times VCU1,2\ [V]$$

The over charge condition is released in two cases:

1) The battery voltage which exceeded the over charge detection voltage (VCU1,2) falls below the over charge release voltage (VCD1,2), the charging FET turns on and the normal condition returns.
2) If the battery voltage which exceeded the over charge detection voltage (VCU1,2) is equal or higher than the over charge release voltage (VCD1,2), but the charger is removed, a load is placed, and discharging starts, the charging FET turns on and the normal condition returns.

The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VM terminal voltage decreases by about 0.6 V from the VSS terminal voltage momentarily. The IC detects this voltage (over current detection voltage 1 or higher), releases the over charge condition and returns to the normal condition.

Over discharge condition

If any one of the battery voltages falls below the over discharge detection voltage (VDD1,2) during discharging under normal condition and it continues for the over discharge detection delay time (tDD1,2) or longer, the discharging FET turns off and discharging stops. This condition is called the over discharge condition. When the discharging FET turns off, the VM terminal voltage becomes equal to the VCC voltage and the IC's current consumption falls below the power-down current consumption (IPDN). This condition is called the power-down condition. The VM and VCC terminals are shorted by the Rvcm resistor under the over discharge and power-down conditions.

The power-down condition is canceled when the charger is connected and the voltage between VM and VCC is over current detection voltage 2 or higher. When all the battery voltages becomes equal to or higher than the over discharge release voltage (VDU1,2) in this condition, the over discharge condition changes to the normal condition.

Delay circuits

The over charge detection delay time (tCU1,2), over discharge detection delay time (tDD1,2), and over current detection delay time 1 (tI0V1) are changed with external capacitor (C3).The delay time for over charge and over discharge and over current detection is changed via an external capacitor. Those three detection delay times are consistent with each other, describe as below.

Over charge delay time : Over discharge delay time: Over current delay time = 100 : 10 : 1

The delay times are calculated by the following equations: (Ta=-40 to +85°C)

Over charge detection delay time Min Typ. Max.
tCU[S] =Delay factor (2.500, 4.545, 9.364)×C3 [uF]
Over discharge detection delay time
tDD[S] =Delay factor (0.3045, 0.4545, 0.6409)×C3 [uF]
Over current detection delay time
tIOV1[S]=Delay factor (0.02864, 0.04545, 0.06682)×C3 [uF]

Note: The delay time for over current detection 2 is fixed by an internal IC circuit. The delay time cannot be changed via an external capacitor.

0V battery charging function (*2)

This function is used to recharge both of two serially-connected batteries after they self-discharge to 0V. When the 0V charging start voltage (V0CHA) or higher is applied to between VM and VCC by connecting the charger, the charging FET gate is fixed to VCC potential.

When the voltage between the gate sources of the charging FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging FET turns on to start charging. At this time, the discharging FET turns off and the charging current flows through the internal parasitic diode in the discharging FET. If all the battery voltages become equal to or higher than the over discharge release voltage (VDU1,2), the normal condition returns.

0V battery charge inhibiting function (*2)

This function is used to inhibit charge any one of the connected battery after it self-discharge to 0V or shorted internally. At least one of the battery voltage 0.7V or lower, the charging FET gate is fixed to EB- potential.

If the both battery voltages become 0.7V or higher, the charging FET gate turns on.

4.7MΩ resistor is required between CO terminal and EB- terminal. Please refer figure 6.

(*1)

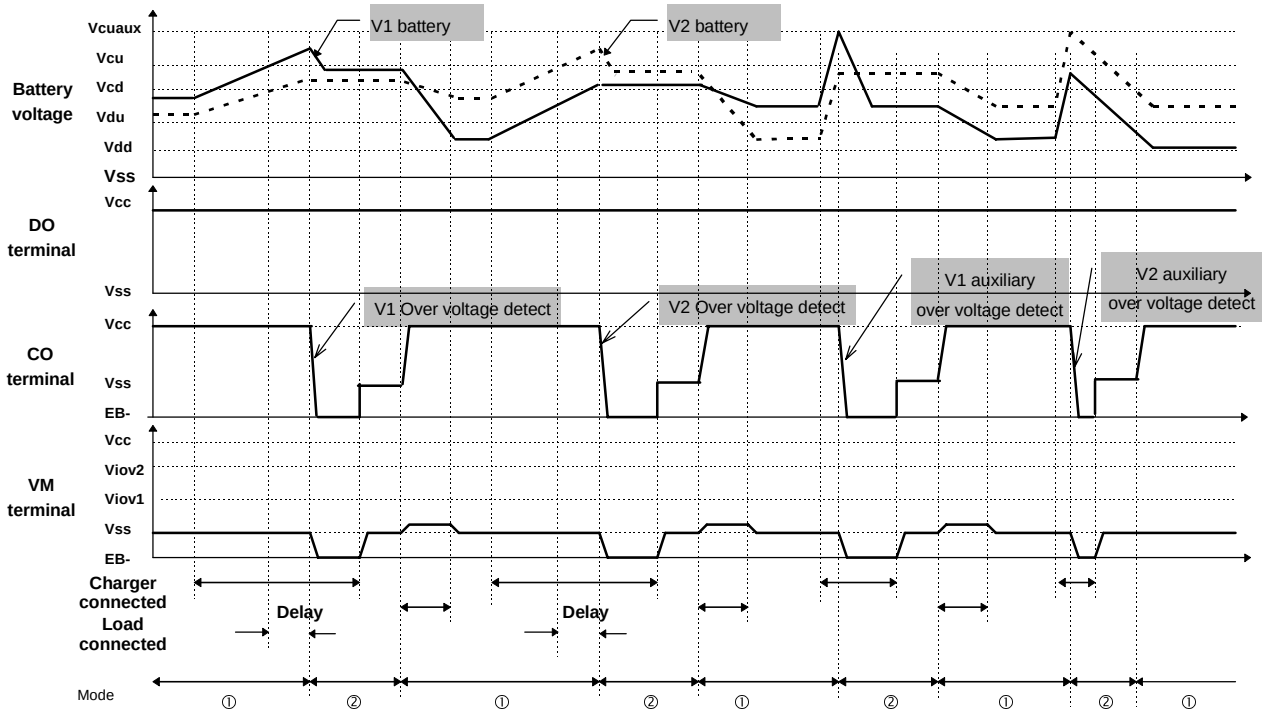
If any one of the battery voltages is equal to or lower than the over discharge release voltage (VDU1,2) when they are connected for the first time, the normal condition may not be entered. If the VMP terminal voltage is made equal to or lower than the VSS voltage (if a charger is connected), the normal condition is entered.

(*2)

Some battery provider doesn't recommend charge for 0V batteries(complete self-discharged). Please refer to battery provider.

■ Operation Timing Charts

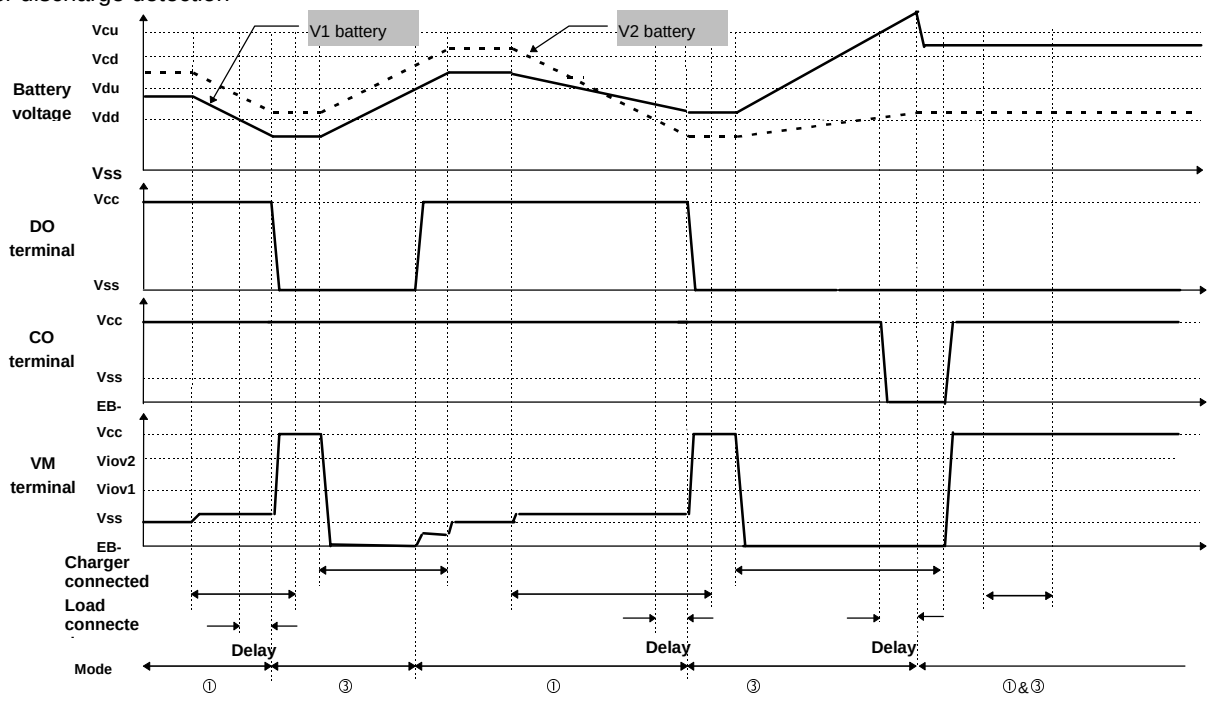
1. Over charge detection



Note: ①Normal mode, ②Over charge mode, ③Over discharge mode, ④over current mode
The charger is assumed to charge with a constant current.

Figure 3

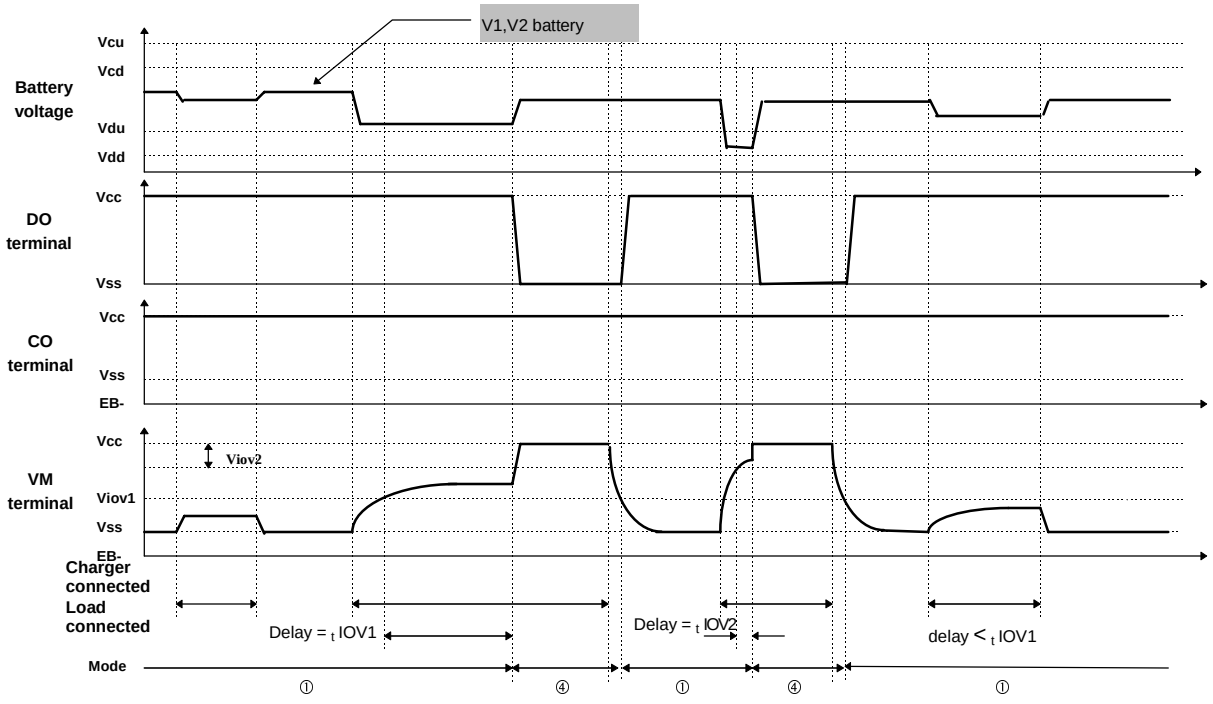
2. Over discharge detection



Note: ①Normal mode, ②Over charge mode,③Over discharge mode, ④over current mode
The charger is assumed to charge with a constant current.

Figure 4

3. Over current detection



Note: ①Normal mode, ②Over charge mode,③Over discharge mode, ④over current mode
The charger is assumed to charge with a constant current.

Figure 5

■ Battery Protection IC Connection Example

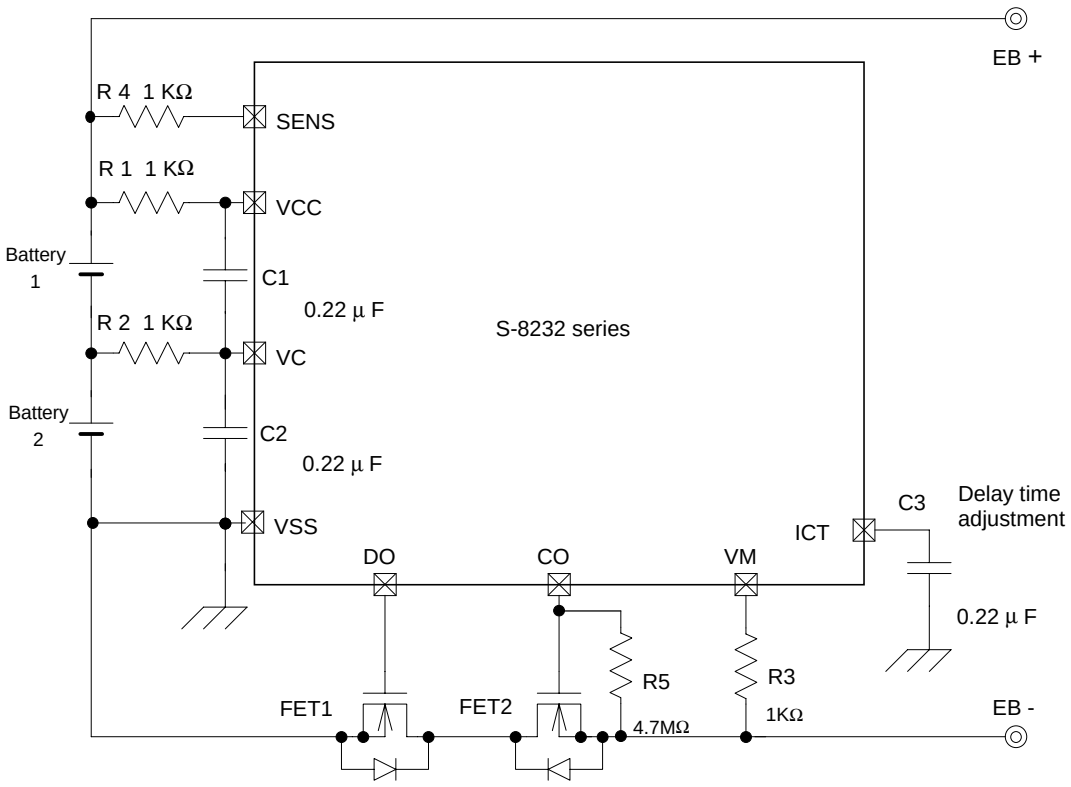


Figure 6

Table 7 Constant

Symbol	Parts	Purpose	Recommend	min.	max.	Remarks
FET1	Nch MOSFET	Charge control	-----	-----	-----	-----
FET2	Nch MOSFET	Discharge control	-----	-----	-----	-----
R1	Chip resistor	For ESD	1KΩ	300Ω	1KΩ	
C1	Chip capacitor	Filter	0.22μF	0μF	1μF	
R2	Chip resistor	For ESD	1KΩ	300Ω	1KΩ	
C2	Chip capacitor	Filter	0.22μF	0μF	1μF	
R4	Chip resistor	For ESD	1KΩ	=R1min	=R1max	***1)*** Put same value resistor=R1,R2
C3	Chip capacitor	Setting delay time	0.22μF	0μF	1μF	***2)*** Note leak current of C2
R3	Chip resistor	Protection at reverse connecting of a charger	1KΩ	300Ω	5KΩ	***3)*** **Discharge can't be stopped at less than 300**Ω when a charger is connected in reverse.
R5	Chip resistor	0V battery charging prevent	(4.7MΩ)	(1MΩ)	(10MΩ)	***4)*** lower resistor increase current consumption

* 1) R4 =R1 is required. Over charge detection voltage is increased by R4. For example 10KΩ(R4) increase over charge detection voltage by 20mV.
* 2) The over charge detection delay time(tCU), the over discharge detection delay time(tCD), and the over current detection delay time(tIOV) are changed with external capacitor C3. See the electrical characteristics.
* 3) R3 is necessary to protect the IC when the charger is connected in reverse. Connect 300Ωor more.
  But excessive R3 causes increasing of Over current detection voltage 1 (VIOV1).
  Please refer the following formulation.
  Δ VIOV1=(R3+Rvsm)/Rvsm×VIOV1-VIOV1
  Foe example 50kΩ(R3) increase Over current detection voltage 1 (VIOV1=0.100V) by 13mV.
* 4) 4.7M Ω(R5)prevents 0V battery from charging. Current consumption is increased by R5. Please connect R5 for only 0V charging unavailable type.

!Note:
The above connection diagram and constants do not guarantee proper operations. Evaluate your actual application and set constants properly.

■ Precautions

(1) After the over current detection delay, if the battery voltages is equals the over discharge detection voltage(VDD1,2) or lower, the over discharge detection delay time becomes shorter than 10mS(min.). It occurs because capacitor C3 sets all of delay times. (Refer fig.7)

[Cause]

It occurs because capacitor C3 sets all of delay times. When over current detection is released until tIOV1 , the capacitor C3 is been charging by S-8232. IF all batteries voltage is lower than VDD1,2 at that time, charging goes on. So delay time is shorter then typical.

[Conclusion]

This phenomenon occurs when all batteries voltage is nearly equal to the over discharge voltage(VDD1,2) after over current detected. It means that the batteries capacity is small and those must be charged in the future. Even if the state change to over discharge condition , the battery package capacity is same as typical.

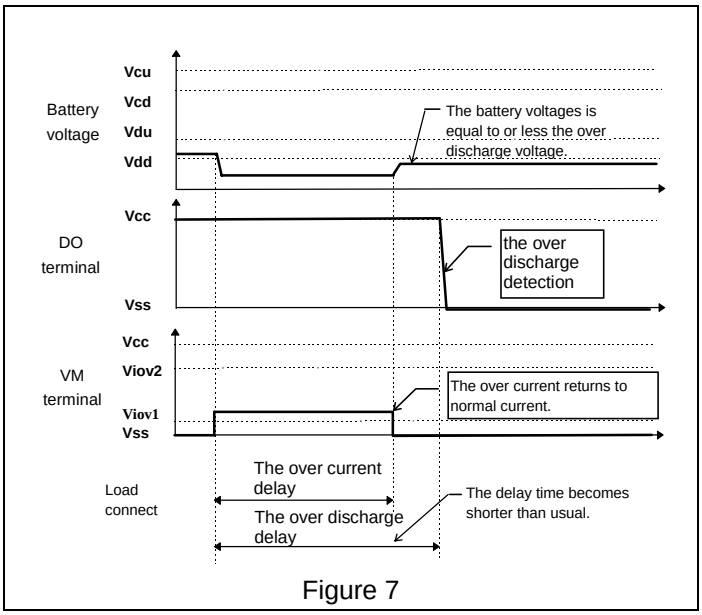


Figure 7

(2) When one of the battery voltages is over discharge detection voltage(VDD1,2) or lower and the other one becomes higher than the over charge detection voltage(VCU1,2), the IC detects the over charge without the over charge detection delay time(tCU). (Refer fig.8)

[Cause]

It is same as the over discharge detection under the over current condition. It occurs because capacitor C3 sets all of delay times.

[Conclusion]

This phenomenon occurs when one battery voltage is lower than over discharge voltage(VDD1,2) and batteries are charged by charger. Under this situation voltage difference between two batteries is unusual. With out delay time is better than long delay time for battery pack safety.(Refer fig.8)

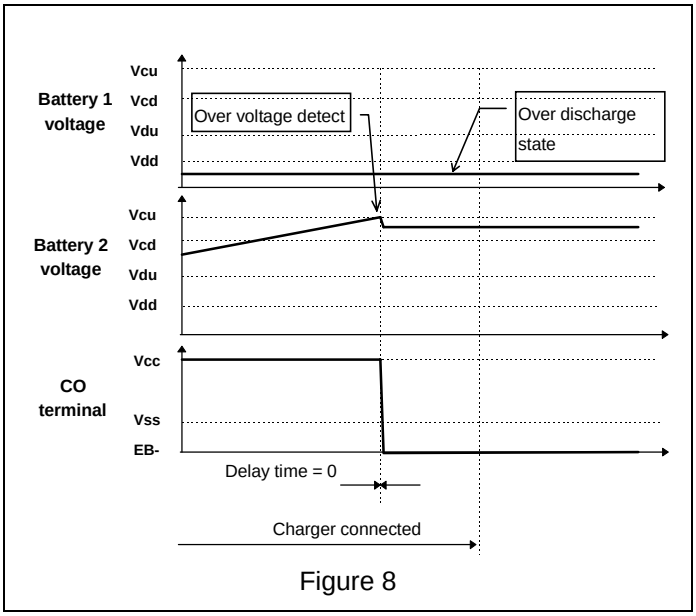


Figure 8

(3) After the over current detection, the load was connected for a long time, even if one of the battery voltage became lower than over discharge detection voltage (VDD1,2), the IC can't detects the over discharge as long as the load is connected. Therefor the IC's current consumption at the one of the battery voltage is lower than the over discharge detection voltage is same as normal condition current consumption (IOPE) . (Refer fig.9)

[Cause]

The reason is as follows. If the over current detection and over discharge detection occur at same time, the over current detection takes precedence the over discharge detection.
As long as the IC detects over current, the IC can't detect over discharge.

[Conclusion]

If the load take off at least one time, the over current release and the over discharge detection works.
Unless keep the IC(S-8232) with load for a long time, the reduction of battery voltage will be neglected, because of the IC's(S-8232) current consumption(typ. 7.5uA) is small.

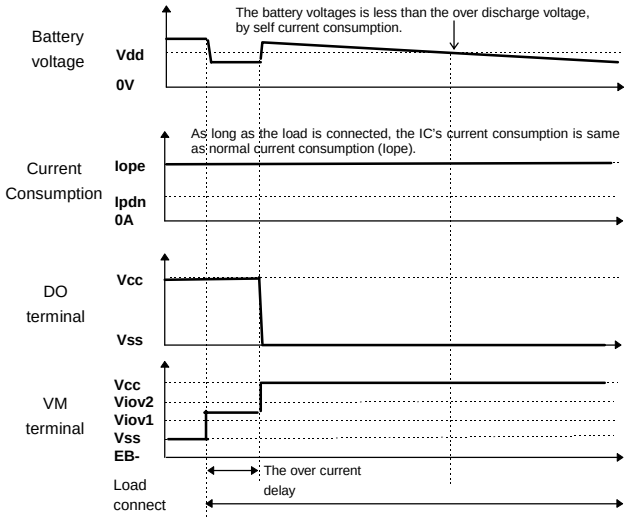


Figure 9

■ Dimensions

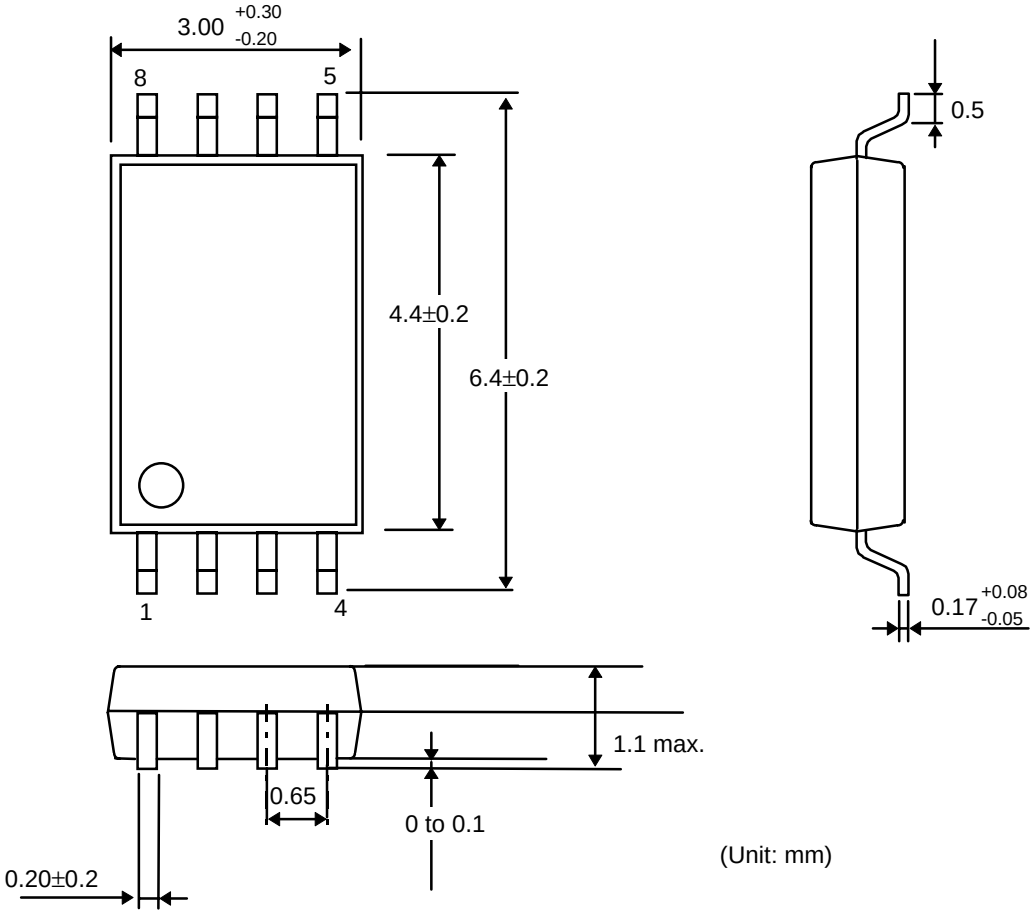
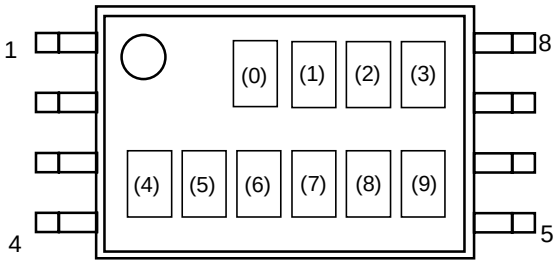


Figure 10

■ Markings



(0) : [A] fix
(1) : [T] fix
(2) : Assembly year (last digit of the year)
(3) : Assembly month(1to9,X,Y,Z)
(4) to (9): Product name

Figure 11

■ Taping

1. Tape specifications

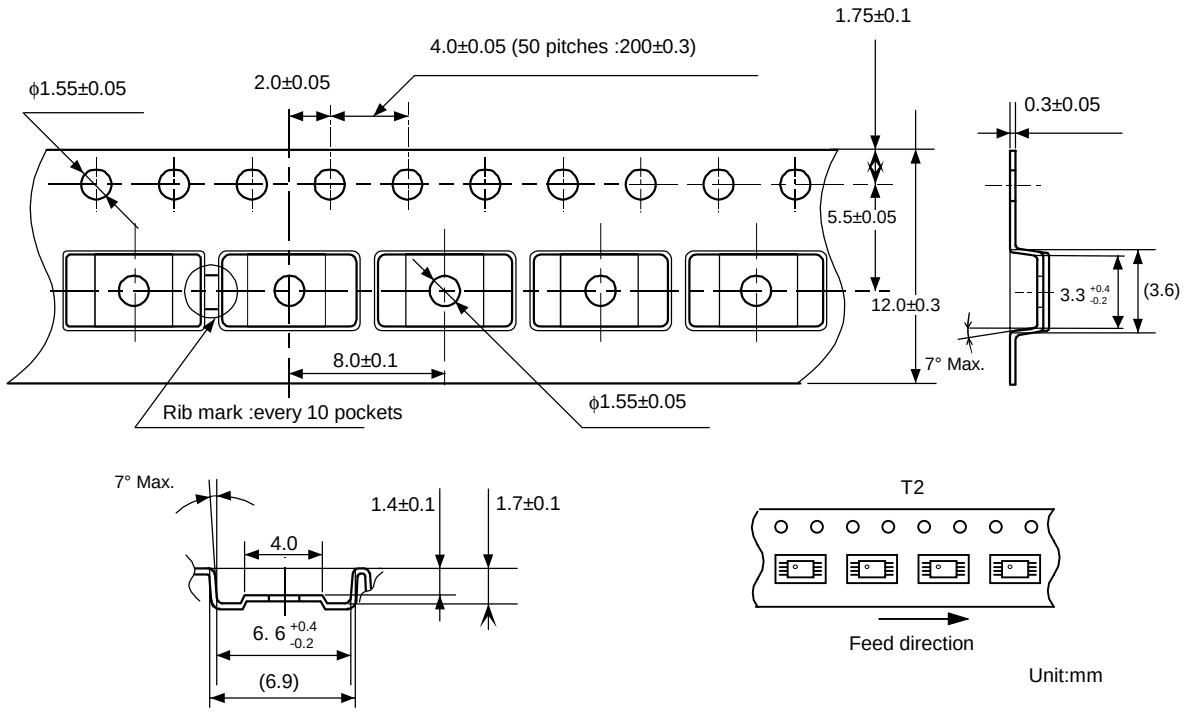


Figure 12

2. Reel specifications

One reel holds 3000 ICs.

External reel diameter

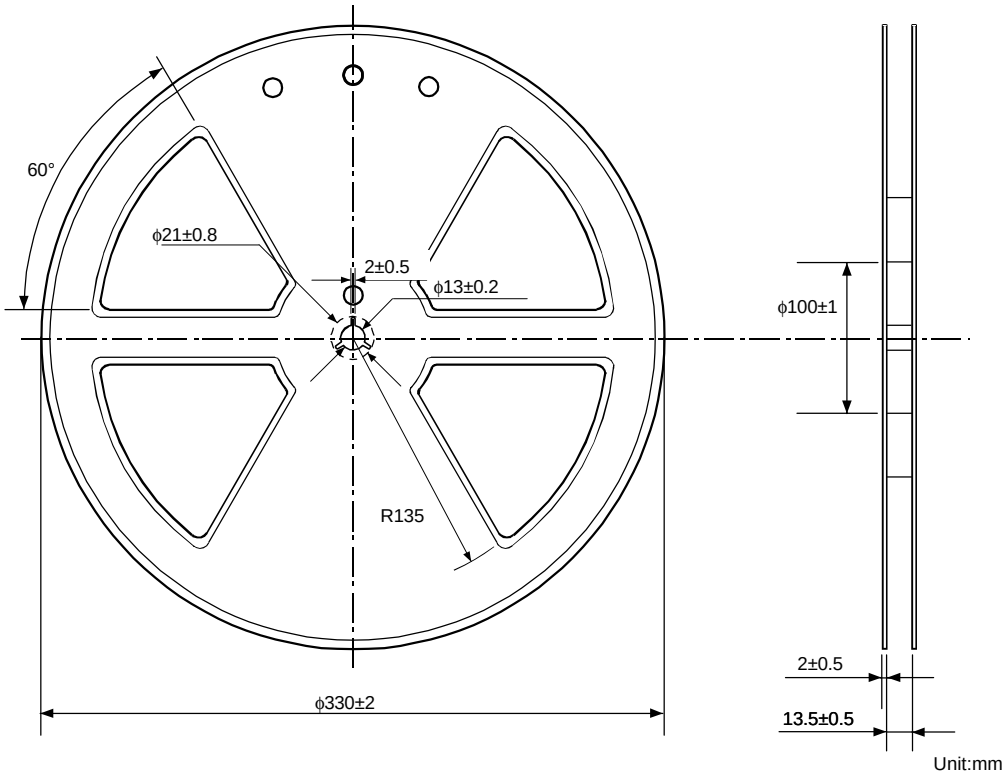
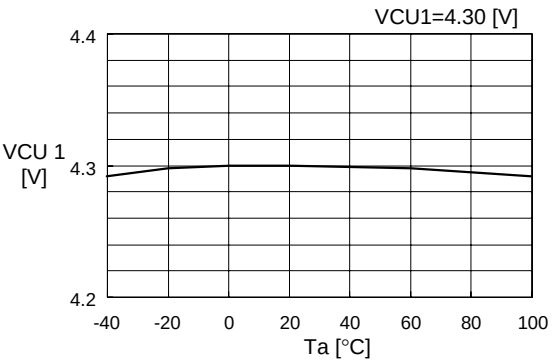


Figure 13

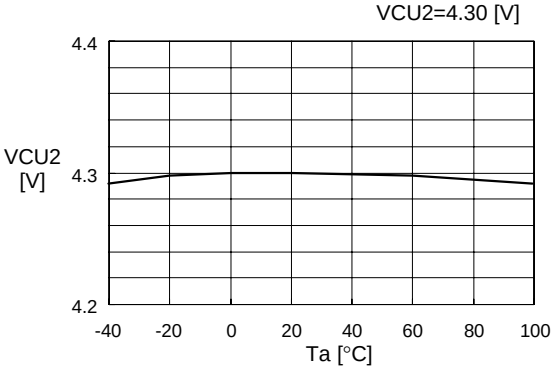
■ Characteristics(typical characteristics)

1. Detection voltage temperature characteristics

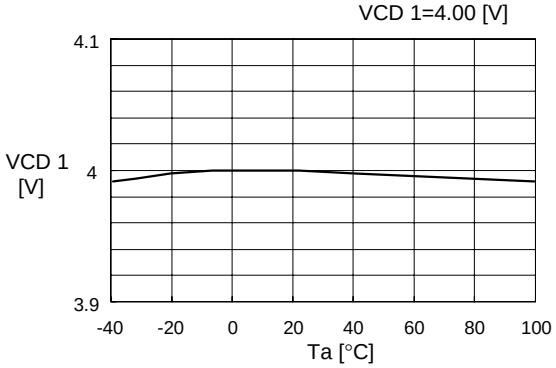
Over charge detection voltage1 vs.temperature



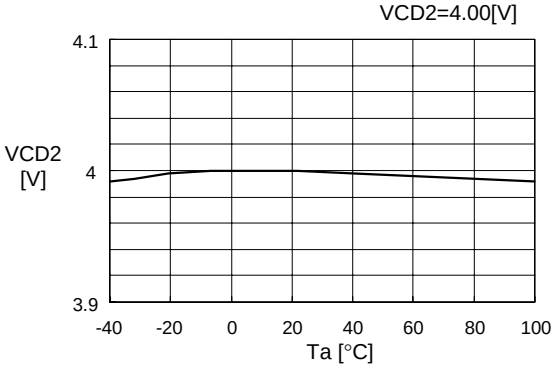
Over charge detection voltage2 vs.temperature



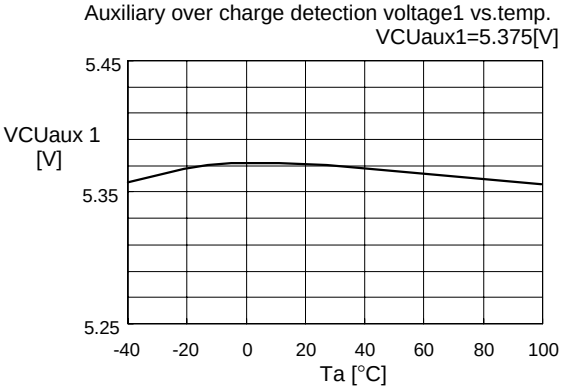
Over charge release voltage1 vs.temperature



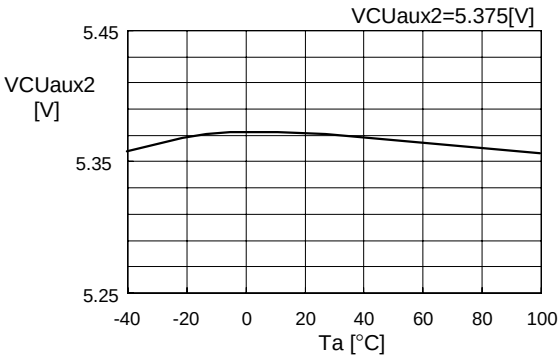
Over charge release voltage2 vs.temperature



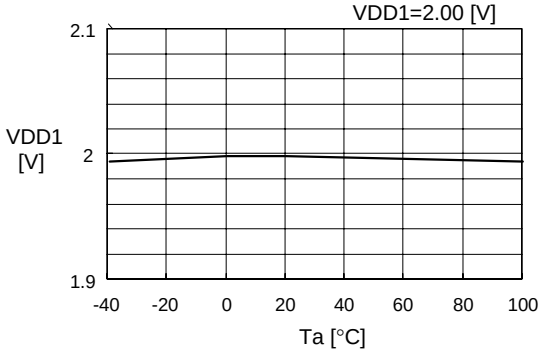
Auxiliary over charge detection voltage1 vs.temp.



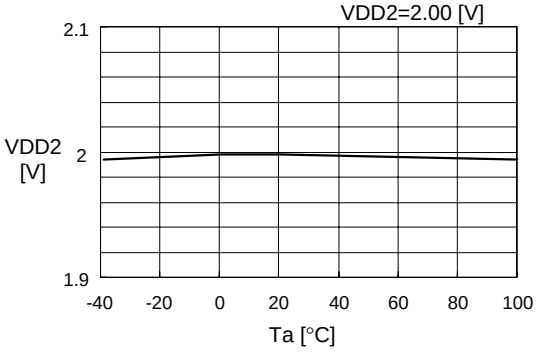
Auxiliary over charge detection voltage2 vs.temp.



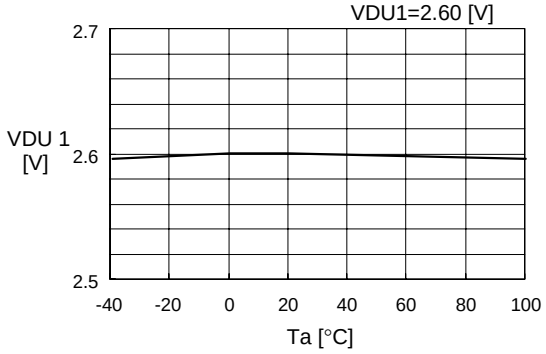
Over discharge detection voltage1 vs.temperature
VDD1=2.00 [V]



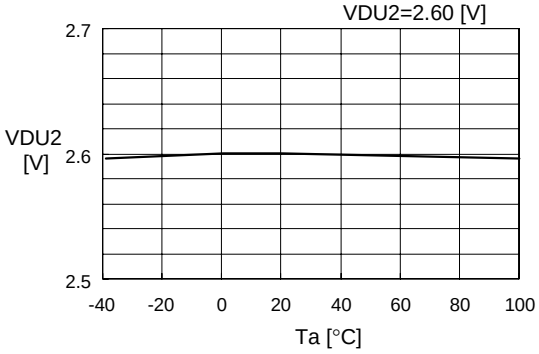
Over discharge detection voltage2 vs.temperature
VDD2=2.00 [V]



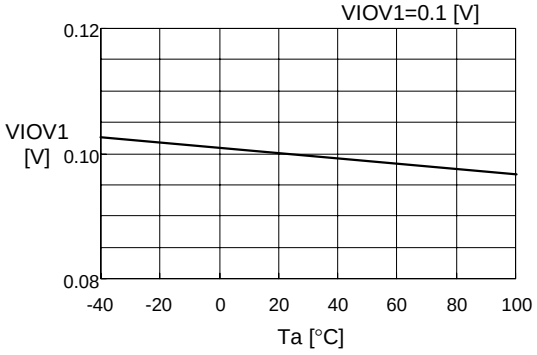
Over discharge release voltage1 vs.temperature
VDU1=2.60 [V]



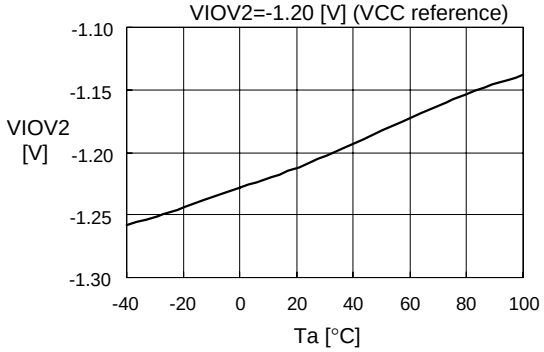
Over discharge release voltage1 vs.temperature
VDU2=2.60 [V]



Over current1 detection voltage vs.temperature
VIOV1=0.1 [V]

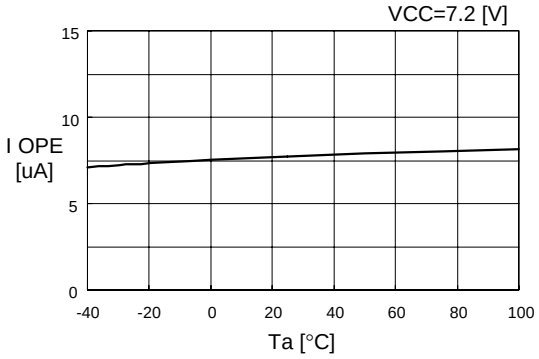


Over current1 detection voltage vs.temperature
VIOV2=-1.20 [V] (VCC reference)

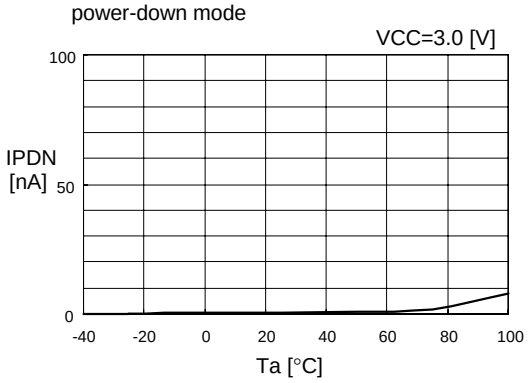


2.Current consumption temperature characteristics

Current consumption vs. temperature in normal mode

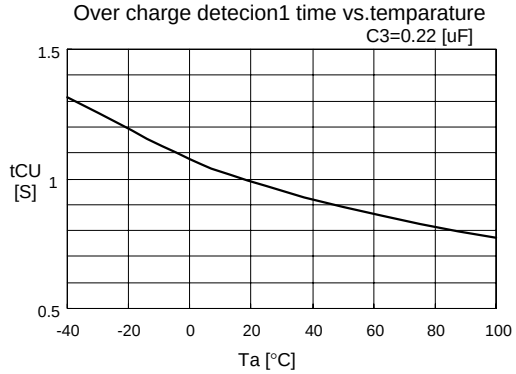


Current consumption vs. temperature in power-down mode

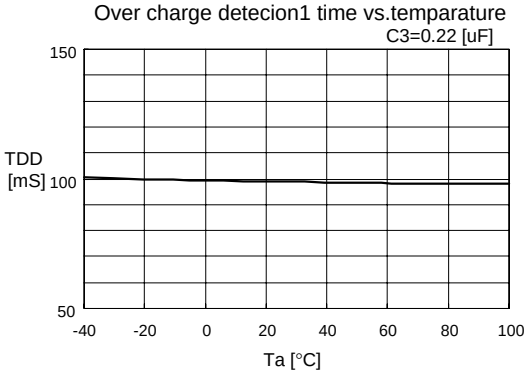


3. Delay time temperature characteristics

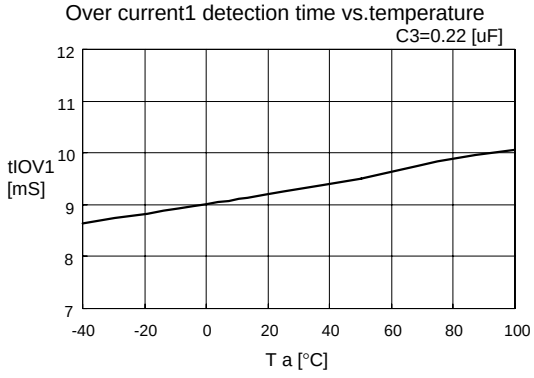
Over charge detecion1 time vs.temparature



Over charge detecion1 time vs.temparature



Over current1 detection time vs.temperature



* Please design all applications of the S-8232 Series with safety in mind.