Protection for Lithium-Ion Batteries (2-serial cells)
Monolithic IC MM3112 Series

Outline

This IC integrates overcharge/overdischarge protection functions for lithium-ion/lithium polymer rechargeable batteries and the regulator functions into one chip by high voltage CMOS process. It can be used with other gas gauge IC, security IC, etc. as it includes a regulator. Overcharge/overdischarge can be detected to protect 2-cell lithium-ion/lithium polymer batteries. Charge/discharge control is perfomed using two external Pch MOS FETs.

Features

1. Overcharge detection voltage	Selectable between 4.0~4.5V by 5mV steps Accuracy ±25mV
2. Overdischarge detection voltage	Selectable between 2.0~3.0V by 100mV steps Accuracy ±80mV
3. No external capacitor for delay time required (delay time is set by the internal circuit)	
4. Regulator output voltage	Selectable between 2.0~4.0V by 0.2V steps Accuracy ±3%
5. Regulator load current	100mA max.
6. Operating temperature range	-40~85°C

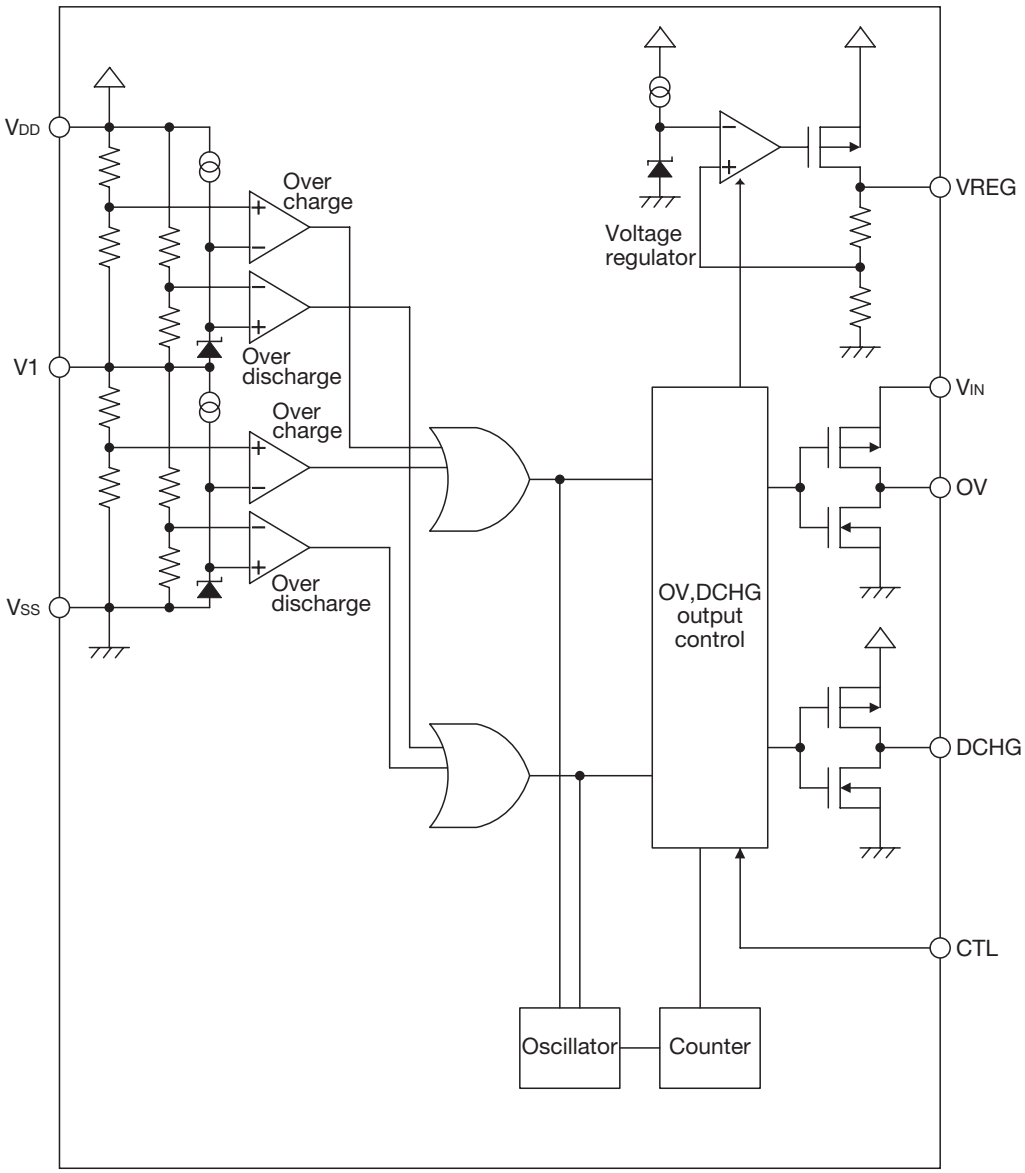
Package

VSOP-10A

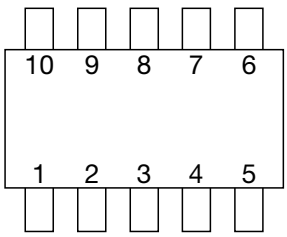
Applications

1. Lithium-ion battery pack (two cells).

Block Diagram



Pin Assignment



VSOP-10A
(TOP-VIEW)

1	DCHG
2	V_{DD}
3	V1
4	V_{SS}
5	V_{SS}
6	V_{SS}
7	VREG
8	CTL
9	V_{IN}
10	OV

Pin Description

Pin No.	Symbol	I/O	Function
1	DCHG	Output	Output of over discharge detection. Output type is CMOS. · Normal mode : "Low" · Overdischarge mode : "High"
2	V_{DD}	Input	The input terminal of the power supply of IC, and the positive voltage of V2 cell.
3	V1	Input	The input terminal of the positive voltage of V1 cell, and the negative voltage of V2 cell .
4	V_{SS}	Input	The input terminal of the ground of IC, and the negative voltage of V1 cell.
5	V_{SS}	Input	The input terminal of the ground of IC, and the negative voltage of V1 cell.
6	V_{SS}	Input	The input terminal of the ground of IC, and the negative voltage of V1 cell.
7	VREG	Output	The output terminal of a voltage regulator. (3.3V) .
8	CTL	Input	The control terminal of FET for charge, and FET for discharge. · CTL= "Low" : DCHG= "Low" Normal mode : OV= "Low" Normal mode · CTL= "High" or "Open" : DCHG= "High" discharge prohibition : OV= "High" charge prohibition
9	V_{IN}	Input	The input terminal of the charger voltage.
10	OV	Output	Output of over charge detection. Output type is CMOS. · Normal mode : "Low" · Overcharge mode : "High"

Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−55~+125	°C
Operating temperature	T_{OPR}	−40~+85	°C
Supply voltage	$V_{DD\ max.}$	V_{SS}−0.3~V_{SS}+24	V
V_{IN} pin supply voltage	$V_{VIN\ max.}$	V_{SS}−0.3~V_{SS}+24	V
OV pin supply voltage	$V_{OV\ max.}$	V_{SS}−0.3~V_{IN}+24	V
DCHG pin supply voltage	$V_{DCHG\ max.}$	V_{SS}−0.3~V_{DD}+0.3	V
CTL pin supply voltage	$V_{CTL\ max.}$	V_{SS}−0.3~V_{DD}+0.3	V
Allowable loss	Pd	300	mW

Recommended Operating Conditions

Item	Symbol	Ratings	Units
Operating temperature	T_{OPR}	−40~+85	°C
Supply voltage	V_{OPR}	V_{SS}+2.0~V_{SS}+18	V

Electrical Characteristics (Except where noted otherwise Ta=+25°C, V_{IN}=V_{DD}, V_{CELL}=3.5V)

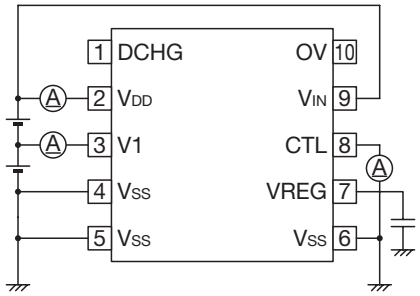
Item	Symbol	Measurement conditions	Min.	Typ.	Max.	Units	Circuit *2
Consumption current	I_{DD}	V_{CELL}=3.5V, I_{OUT}=0mA		10	20	µA	A
Current consumption at stand-by	I_S	V_{CELL}=1.8V, I_{OUT}=0mA			0.1	µA	B
Pin5 (V1) input current	I_{V1}	V_{CELL}=3.5V			±300	nA	A
Overcharge detection voltage	$V_{CELL}U$	Ta=0~+50°C *1 V_{CELL}=3.5V→4.5V	4.325	4.35	4.375	V	C
Overcharge releasee voltage	$V_{CELL}O$	V_{CELL}=4.5V→3.5V	$V_{CELL}U$ −260mV	$V_{CELL}U$ −200mV	$V_{CELL}U$ −140mV	V	C
Overcharge detection dead time	t_{OV}	V_{CELL}=3.5V→4.5V	50	100	150	ms	C
Overcharge release dead time	t_{OVREL}	V_{CELL}=4.5V→3.5V	10	20	40	ms	C
Overdischarge detection voltage	$V_{CELL}S$	V_{CELL}=3.5V→1.8V	2.22	2.3	2.38	V	D
Overdischarge release voltage	$V_{CELL}D$	V_{IN}=V_{DD} V_{CELL}=1.8V→3.5V	2.7	2.8	2.9	V	D
Overdischarge detection dead time	t_{DC}	V_{CELL}=3.5V→1.8V	15	30	45	ms	D
Overdischarge release dead time	t_{DCREL}	V_{CELL}=1.8V→3.5V	10	20	40	ms	D
Pin1 (DCHG) source current	$I_{SO}D_{CH}$	V_{CELL} < $V_{CELL}S$ V_{DCHG}=V_{DD}−0.5V	20			µA	E
Pin1 (DCHG) sink current	$I_{SI}D_{CH}$	V_{DCHG}=0.5V	20			µA	F
Pin1 (DCHG) output voltage H	$V_{TH}D_{CH}$	V_{CELL} < $V_{CELL}S$ V_{DD}−V_{DCHG} I_{SO}=20µA			0.5	V	E
Pin1 (DCHG) output voltage L	$V_{TH}D_{CL}$	V_{DCHG}−V_{SS} I_{SI}=−20µA			0.5	V	F
Pin10 (OV) source current	$I_{SO}O_V$	V_{CELL} < $V_{CELL}U$ V_{OV}=V_{IN}−0.5V	20			µA	G
Pin10 (OV) sink current	$I_{SI}O_V$	V_{OV}=0.5V Ta=−40~85°C *1	20			µA	F
Pin10 (OV) output voltage H	$V_{TH}O_VH$	V_{CELL} < $V_{CELL}U$ V_{IN}−V_{OV} I_{SO}=20µA			0.5	V	G
Pin10 (OV) output voltage L	$V_{TH}O_VL$	V_{OV}−V_{SS} I_{SI}=−20µA Ta=−40~85°C *1			0.5	V	F
Pin7 (CTL) High current	I_{CTLH}	V_{CELL}=3.5V, V_{CTL}=V_{DD}			0.1	µA	H
Pin7 (CTL) Low current	I_{CTLL}	V_{CELL}=3.5V, V_{CTL}=V_{SS}	−3	−1.7		µA	A
Pin7 (CTL) High voltage	V_{CTLH}		V_{DD} ×0.8			V	I
Pin7 (CTL) Low voltage	V_{CTLL}				0.5	V	I
Pin8 (VREG) output voltage	V_{OUT}	V_{CELL}=3.5V, I_{OUT}=1mA	3.221	3.300	3.379	V	J
Pin8 (VREG) line regulation	ΔV_{OUT1}	V_{CELL}=2.4V→6V, I_{OUT}=1mA		5	15	mV	J
Pin8 (VREG) load regulation	ΔV_{OUT2}	V_{CELL}=3.5V, I_{OUT}=1→20mA		40	80	mV	J

*1 : The parameter is guaranteed by design.

*2 : The test circuit symbols on next page.

Measuring Circuit

A



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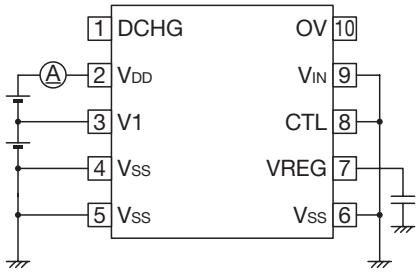

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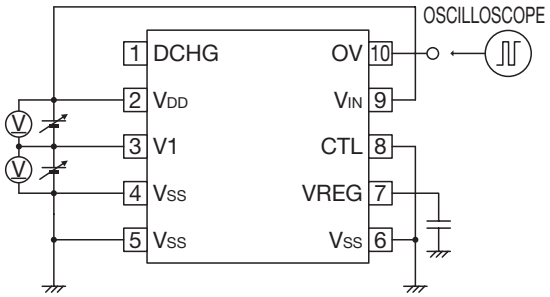

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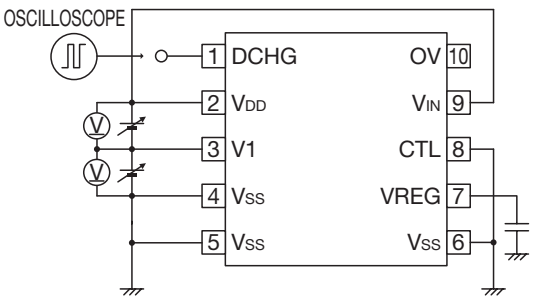

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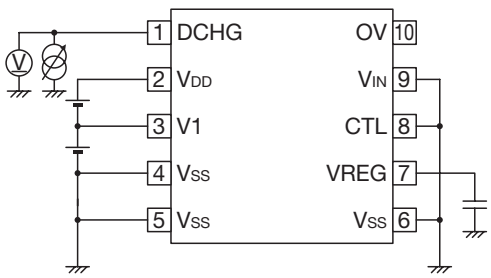

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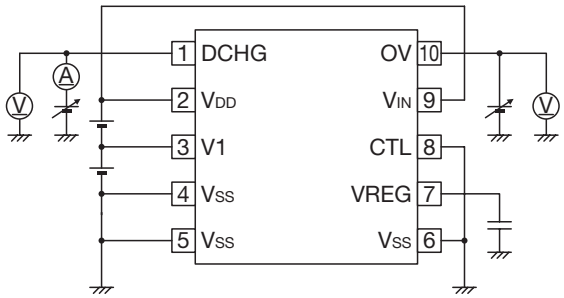

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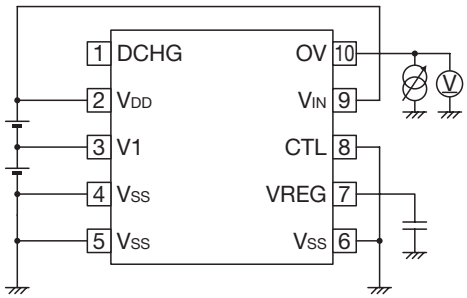

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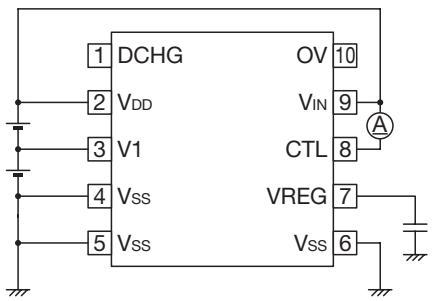

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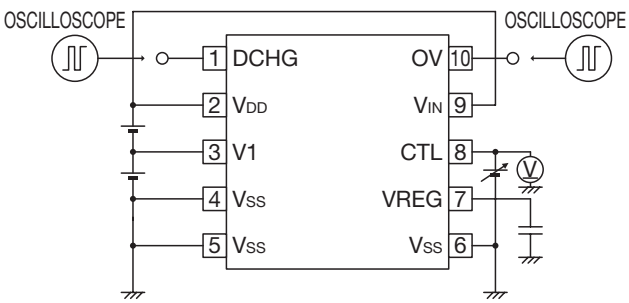

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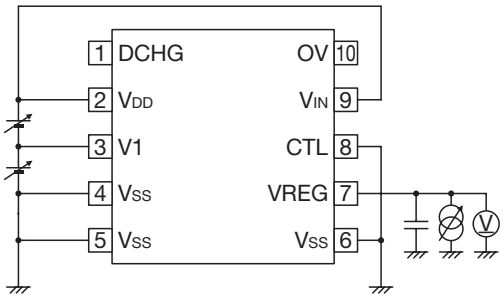
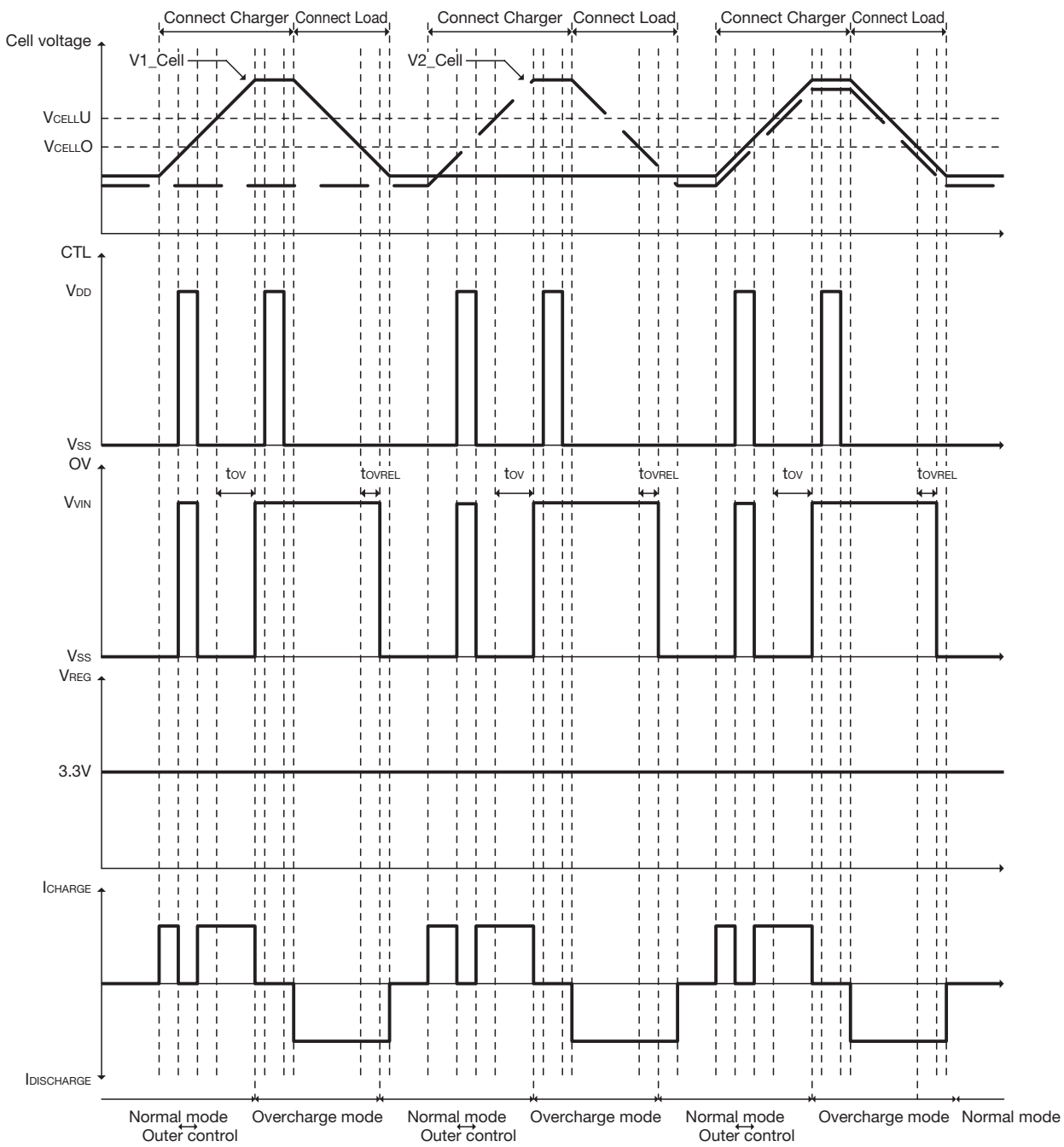
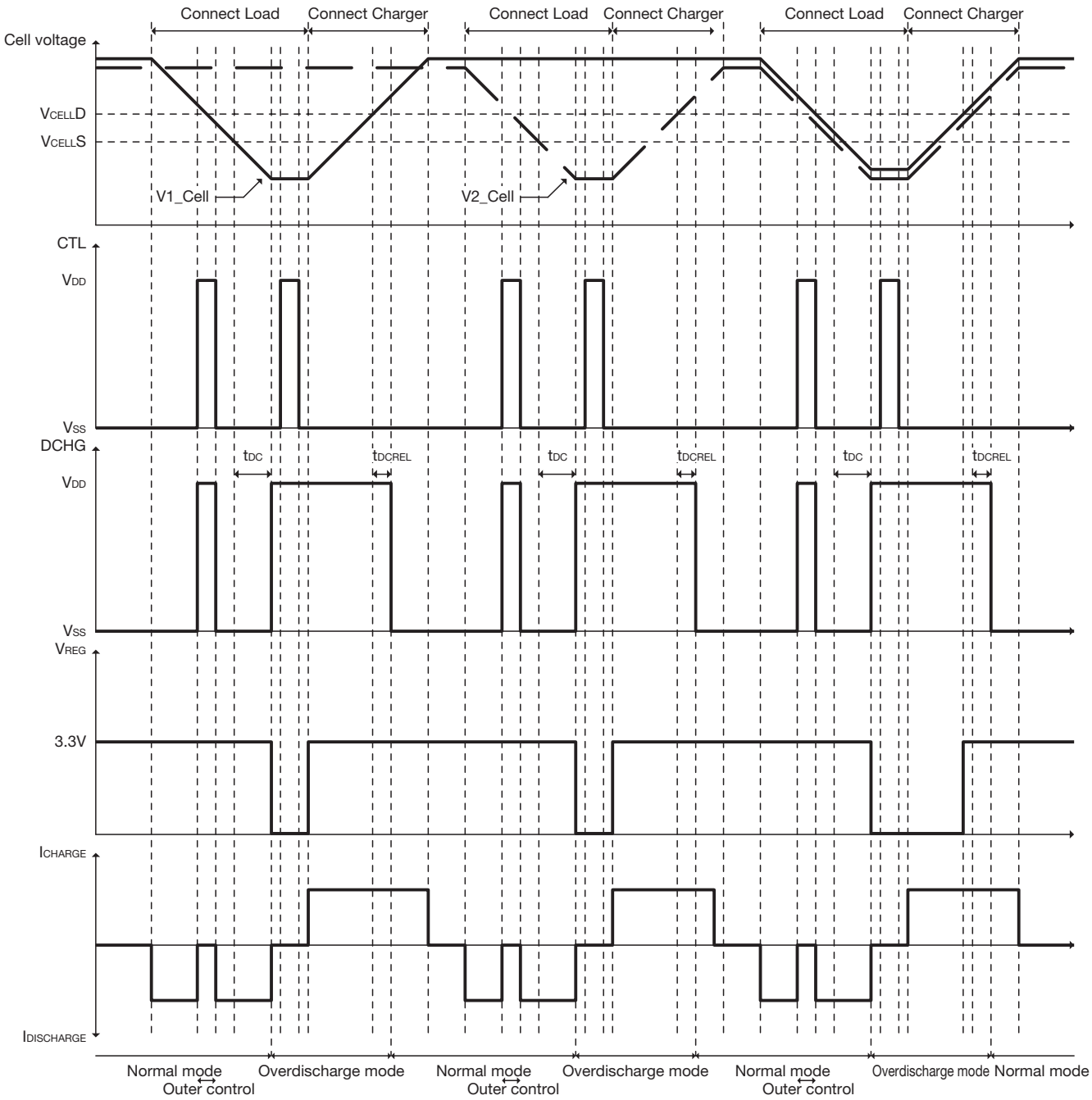


Timing chart

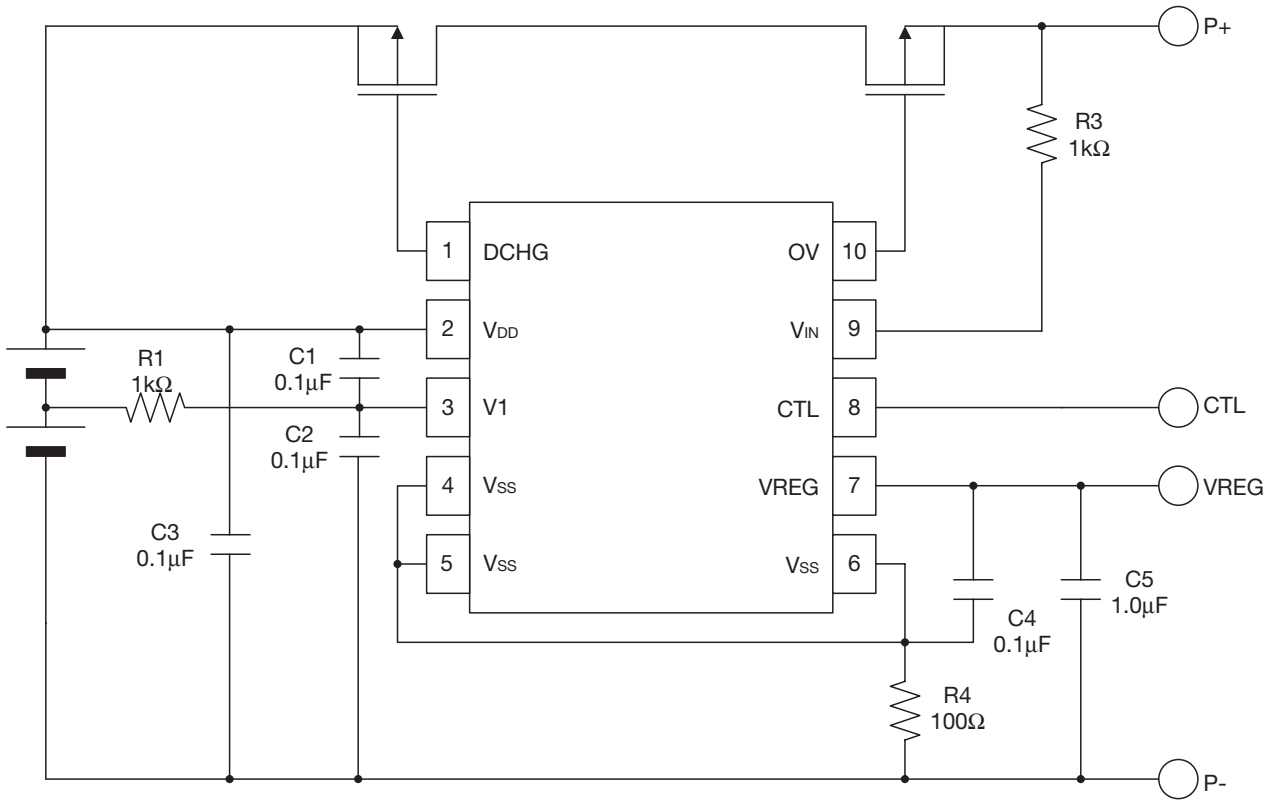
Overchage Function



Overdischage Function



Application Circuit



· These circuits are typical examples provided for reference purposes, so in actual applications, the circuit constants, conditions and operations should be thoroughly studied.

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