# S-8200A Series

## BATTERY PROTECTION IC FOR 1-CELL PACK

www.sii-ic.com



Rev.3.0_00

The S-8200A Series is a protection IC for single-cell lithium-ion / lithium polymer rechargeable batteries and include high-accuracy voltage detectors and delay circuits.
The S-8200A Series is suitable for protecting single-cell rechargeable lithium-ion / lithium polymer battery packs from overcharge, overdischarge, and overcurrent.

## ■ Features

- High-accuracy voltage detection circuit

| | | |
|---|---|---|
| Overcharge detection voltage | 3.5 V to 4.5 V (5 mV steps) | Accuracy ±20 mV (Ta = +25°C) |
| | | Accuracy ±25 mV (Ta = −10°C to +60°C) |
| Overcharge release voltage | 3.1 V to 4.5 V*1 | Accuracy ±30 mV |
| Overdischarge detection voltage | 2.0 V to 3.4 V (10 mV steps) | Accuracy ±35 mV |
| Overdischarge release voltage | 2.0 V to 3.4 V*2 | Accuracy ±50 mV |
| Discharge overcurrent detection voltage | 0.05 V to 0.20 V (10 mV steps) | Accuracy ±10 mV |
| Load short-circuiting detection voltage | 0.5 V (fixed) | Accuracy ±100 mV |
| Charge overcurrent detection voltage | −0.20 V to −0.05 V (25 mV steps) | Accuracy ±15 mV |

- Detection delay times are generated by an internal circuit (external capacitors are unnecessary).
  Accuracy ±20%
- High-withstanding-voltage device is used for charger connection pins
  (VM pin and CO pin : Absolute maximum rating = 28 V)
- 0 V battery charge function available / unavailable are selectable.
- Selectable power-down function available / unavailable.
- Wide operating temperature range Ta = −40°C to +85°C
- Low current consumption

| | |
|---|---|
| Operation mode | 2.8 μA typ., 5.0 μA max. (Ta = +25°C) |
| Power-down mode | 0.1 μA max. (Ta = +25°C) |

- Lead-free (Sn 100%), halogen-free*3

***1.** Overcharge release voltage = Overcharge detection voltage − Overcharge hysteresis voltage
(Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV steps.)
***2.** Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage
(Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV steps.)
***3.** Refer to the "■ **Product Name Structure**" for details.

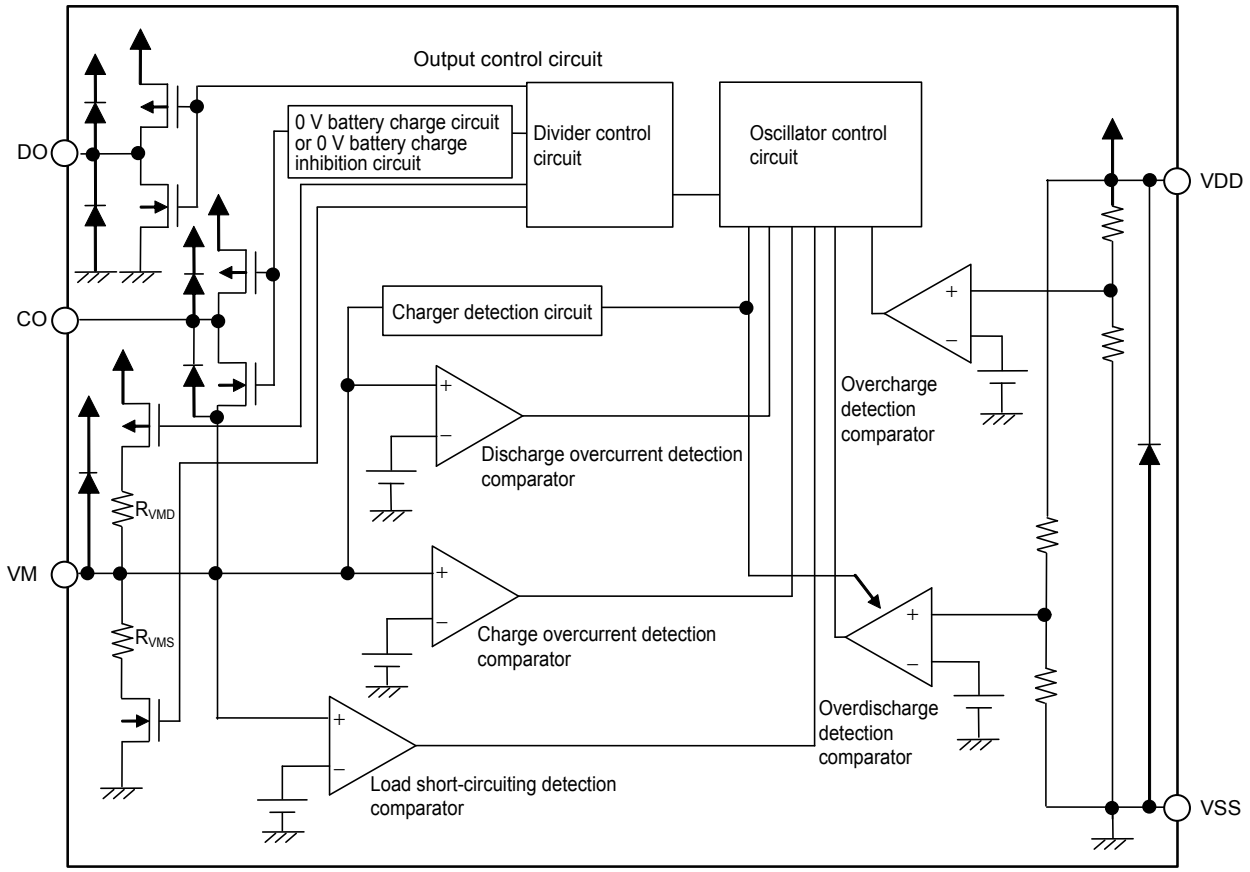
## ■ Applications

- Lithium-ion rechargeable battery packs
- Lithium polymer rechargeable battery packs

## ■ Packages

- SOT-23-6
- SNT-6A

## ■ Block Diagram

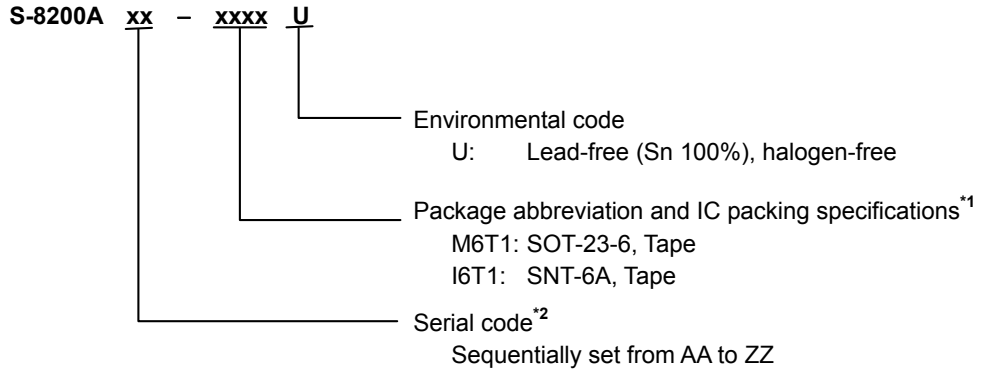



**Remark** All diodes shown in figure are parasitic diodes.

**Figure 1**

## ■ Product Name Structure

### 1. Product Name




***1.** Refer to the tape specifications.
***2.** Refer to the "**3. Product Name List**".

### 2. Packages

| Package Name | Drawing Code | | | |
|---|---|---|---|---|
| | Package | Tape | Reel | Land |
| SOT-23-6 | MP006-A-P-SD | MP006-A-C-SD | MP006-A-R-SD | – |
| SNT-6A | PG006-A-P-SD | PG006-A-C-SD | PG006-A-R-SD | PG006-A-L-SD |

### 3. Product Name Lists

#### 3. 1 SOT-23-6

**Table 1**

| Product Name | Overcharge Detection Voltage [$V_{CU}$] | Overcharge Release Voltage [$V_{CL}$] | Over-discharge Detection Voltage [$V_{DL}$] | Over-discharge Release Voltage [$V_{DU}$] | Discharge Overcurrent Detection Voltage [$V_{DIOV}$] | Charge Overcurrent Detection Voltage [$V_{CIOV}$] | 0 V Battery Charge Function | Delay Time Combination*1 | Power-down Function |
|---|---|---|---|---|---|---|---|---|---|
| S-8200AAC-M6T1U | 4.225 V | 4.025 V | 2.500 V | 2.900 V | 0.150 V | –0.150 V | Available | (1) | Unavailable |

***1.** Refer to the **Table 3** about the details of the delay time combinations.

#### 3. 2 SNT-6A

**Table 2**

| Product Name | Overcharge Detection Voltage [$V_{CU}$] | Overcharge Release Voltage [$V_{CL}$] | Over-discharge Detection Voltage [$V_{DL}$] | Over-discharge Release Voltage [$V_{DU}$] | Discharge Overcurrent Detection Voltage [$V_{DIOV}$] | Charge Overcurrent Detection Voltage [$V_{CIOV}$] | 0 V Battery Charge Function | Delay Time Combination*1 | Power-down Function |
|---|---|---|---|---|---|---|---|---|---|
| S-8200AAA-I6T1U | 4.225 V | 4.025 V | 2.500 V | 2.900 V | 0.150 V | –0.150 V | Unavailable | (1) | Available |
| S-8200AAB-I6T1U | 4.250 V | 4.050 V | 2.400 V | 2.900 V | 0.050 V | –0.100 V | Unavailable | (1) | Available |
| S-8200AAC-I6T1U | 4.225 V | 4.025 V | 2.500 V | 2.900 V | 0.150 V | –0.150 V | Available | (1) | Unavailable |
| S-8200AAD-I6T1U | 4.275 V | 4.075 V | 2.600 V | 2.600 V | 0.120 V | –0.100 V | Available | (2) | Available |
| S-8200AAF-I6T1U | 4.225 V | 4.025 V | 2.800 V | 2.800 V | 0.150 V | –0.150 V | Unavailable | (1) | Available |

***1.** Refer to the **Table 3** about the details of the delay time combinations.

**Remark** Please contact our sales office for the products with detection voltage value other than those specified above.

**Table 3**

| Delay Time Combination | Overcharge Detection Delay Time [$t_{CU}$] | Overdischarge Detection Delay Time [$t_{DL}$] | Discharge Overcurrent Detection Delay Time [$t_{DIOV}$] | Load Short-circuiting Detection Delay Time [$t_{SHORT}$] | Charge Overcurrent Detection Delay Time [$t_{CIOV}$] |
|---|---|---|---|---|---|
| (1) | 1.0 s | 64 ms | 8 ms | 250 μs | 8 ms |
| (2) | 1.0 s | 32 ms | 8 ms | 250 μs | 8 ms |

**Remark** The delay times can be changed within the range listed **Table 3**. For details, please contact our sales office.

**Table 4**

| Delay Time | Symbol | Selection Range | | | Remark |
|---|---|---|---|---|---|
| Overcharge detection delay time | $t_{CU}$ | 256 ms | 512 ms | 1.0 s*1 | Select a value from the left. |
| Overdischarge detection delay time | $t_{DL}$ | 32 ms | 64 ms*1 | 128 ms | Select a value from the left. |
| Discharge overcurrent detection delay time | $t_{DIOV}$ | 4 ms | 8 ms*1 | 16 ms | Select a value from the left. |
| Load short-circuiting detection delay Time | $t_{SHORT}$ | 250 μs*1 | 500 μs | 1 ms | Select a value from the left. |
| Charge overcurrent detection delay time | $t_{CIOV}$ | 4 ms | 8 ms*1 | 16 ms | Select a value from the left. |

***1.** This value is the delay time of the standard products.

## ■ Pin Configurations

### 1. SOT-23-6

SOT-23-6
Top view

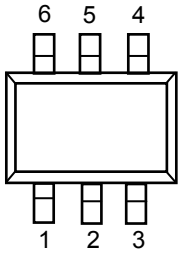



**Figure 2**

**Table 5**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | DO | Connection of discharge control FET gate (CMOS output) |
| 2 | VM | Voltage detection between VM pin and VSS pin (Overcurrent / charger detection pin) |
| 3 | CO | Connection of charge control FET gate (CMOS output) |
| 4 | NC*1 | No connection |
| 5 | VDD | Connection for positive power supply input |
| 6 | VSS | Connection for negative power supply input |

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

### 2. SNT-6A

SNT-6A
Top view

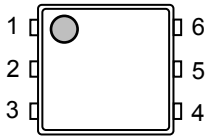



**Figure 3**

**Table 6**

| Pin No. | Symbol | Description |
|---|---|---|
| 1 | NC*1 | No connection |
| 2 | CO | Connection of charge control FET gate (CMOS output) |
| 3 | DO | Connection of discharge control FET gate (CMOS output) |
| 4 | VSS | Connection for negative power supply input |
| 5 | VDD | Connection for positive power supply input |
| 6 | VM | Voltage detection between VM pin and VSS pin (Overcurrent / charger detection pin) |

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD or VSS.

## ■ Absolute Maximum Ratings

**Table 7**

(Ta = +25°C unless otherwise specified)

| Item | | Symbol | Applied pin | Absolute Maximum Ratings | Unit |
|---|---|---|---|---|---|
| Input voltage between VDD pin and VSS pin | | $V_{DS}$ | VDD | $V_{SS}$ − 0.3 to $V_{SS}$ + 12 | V |
| VM pin input voltage | | $V_{VM}$ | VM | $V_{DD}$ − 28 to $V_{DD}$ + 0.3 | V |
| DO pin output voltage | | $V_{DO}$ | DO | $V_{SS}$ − 0.3 to $V_{DD}$ + 0.3 | V |
| CO pin output voltage | | $V_{CO}$ | CO | $V_{VM}$ − 0.3 to $V_{DD}$ + 0.3 | V |
| Power dissipation | SOT-23-6 | $P_D$ | − | 650*1 | mW |
| | SNA-6A | | − | 400*1 | mW |
| Operating ambient temperature | | $T_{opr}$ | − | − 40 to + 85 | °C |
| Storage temperature | | $T_{stg}$ | − | − 55 to + 125 | °C |

***1.** When mounted on board
[Mounted board]
(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm
(2) Board name:JEDEC STANDARD51-7

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

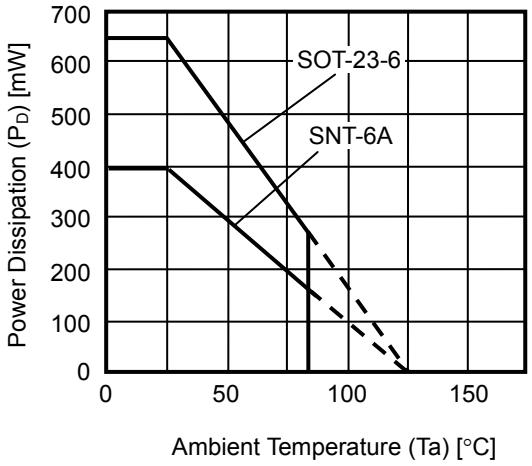



**Figure 4 Power Dissipation of Package (When Mounted on Board)**

## ■ Electrical Characteristics

### 1. Ta = +25°C

**Table 8**

(Ta = +25°C unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|
| **DETECTION VOLTAGE** | | | | | | | |
| Overcharge detection voltage | $V_{CU}$ | – | $V_{CU}$–0.020 | $V_{CU}$ | $V_{CU}$+0.020 | V | 1 |
| | | Ta = −10°C to +60°C*1 | $V_{CU}$–0.025 | $V_{CU}$ | $V_{CU}$+0.025 | V | 1 |
| Overcharge release voltage | $V_{CL}$ | $V_{CL} \neq V_{CU}$ | $V_{CL}$–0.030 | $V_{CL}$ | $V_{CL}$+0.030 | V | 1 |
| | | $V_{CL} = V_{CU}$ | $V_{CL}$–0.025 | $V_{CL}$ | $V_{CL}$+0.020 | V | 1 |
| Overdischarge detection voltage | $V_{DL}$ | – | $V_{DL}$–0.035 | $V_{DL}$ | $V_{DL}$+0.035 | V | 2 |
| Overdischarge release voltage | $V_{DU}$ | $V_{DL} \neq V_{DU}$ | $V_{DU}$–0.050 | $V_{DU}$ | $V_{DU}$+0.050 | V | 2 |
| | | $V_{DL} = V_{DU}$ | $V_{DU}$–0.035 | $V_{DU}$ | $V_{DU}$+0.035 | V | 2 |
| Discharge overcurrent detection voltage | $V_{DIOV}$ | – | $V_{DIOV}$–0.010 | $V_{DIOV}$ | $V_{DIOV}$+0.010 | V | 2 |
| Load short-circuiting detection voltage | $V_{SHORT}$ | – | 0.40 | 0.50 | 0.60 | V | 2 |
| Charge overcurrent detection voltage | $V_{CIOV}$ | – | $V_{CIOV}$–0.015 | $V_{CIOV}$ | $V_{CIOV}$+0.015 | V | 2 |
| **0 V BATTERY CHARGE FUNCTION** | | | | | | | |
| 0 V battery charge starting charger voltage | $V_{0CHA}$ | 0 V battery charging function “available” | 0.0 | 0.7 | 1.0 | V | 2 |
| 0 V battery charge inhibition battery voltage | $V_{0INH}$ | 0 V battery charging function “unavailable” | 0.6 | 0.8 | 1.1 | V | 2 |
| **INTERNAL RESISTANCE** | | | | | | | |
| Resistance between VM pin and VDD pin | $R_{VMD}$ | $V_{DD}$ = 1.8 V, $V_{VM}$ = 0 V | 100 | 300 | 900 | kΩ | 3 |
| Resistance between VM pin and VSS pin | $R_{VMS}$ | $V_{DD}$ = 3.4 V, $V_{VM}$ = 1.0 V | 10 | 20 | 40 | kΩ | 3 |
| **INPUT VOLTAGE** | | | | | | | |
| Operating voltage between VDD pin and VSS pin | $V_{DSOP1}$ | – | 1.5 | – | 6.5 | V | – |
| Operating voltage between VDD pin and VM pin | $V_{DSOP2}$ | – | 1.5 | – | 28 | V | – |
| **INPUT CURRENT (Product with power-down function)** | | | | | | | |
| Current consumption during operation | $I_{OPE}$ | $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 1.0 | 2.8 | 5.0 | μA | 2 |
| Current consumption at power-down | $I_{PDN}$ | $V_{DD}$ = $V_{VM}$ = 1.5 V | – | – | 0.1 | μA | 2 |
| **INPUT CURRENT (Product without power-down function)** | | | | | | | |
| Current consumption during operation | $I_{OPE}$ | $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 1.0 | 2.8 | 5.0 | μA | 2 |
| Current consumption during overdischarge | $I_{OPED}$ | $V_{DD}$ = $V_{VM}$ = 1.5 V | – | – | 3.5 | μA | 2 |
| **OUTPUT RESISTANCE** | | | | | | | |
| CO pin resistance “H” | $R_{COH}$ | $V_{CO}$ = 3.0 V, $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 5 | 10 | 20 | kΩ | 4 |
| CO pin resistance “L” | $R_{COL}$ | $V_{CO}$ = 0.4 V, $V_{DD}$ = 4.6 V, $V_{VM}$ = 0 V | 5 | 10 | 20 | kΩ | 4 |
| DO pin resistance “H” | $R_{DOH}$ | $V_{DO}$ = 3.0 V, $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 5 | 10 | 20 | kΩ | 4 |
| DO pin resistance “L” | $R_{DOL}$ | $V_{DO}$ = 0.4 V, $V_{DD}$ = 1.8 V, $V_{VM}$ = 0 V | 5 | 10 | 20 | kΩ | 4 |
| **DELAY TIME** | | | | | | | |
| Overcharge detection delay time | $t_{CU}$ | – | $t_{CU}$×0.8 | $t_{CU}$ | $t_{CU}$×1.2 | – | 5 |
| Overdischarge detection delay time | $t_{DL}$ | – | $t_{DL}$×0.8 | $t_{DL}$ | $t_{DL}$×1.2 | – | 5 |
| Discharge overcurrent detection delay time | $t_{DIOV}$ | – | $t_{DIOV}$×0.8 | $t_{DIOV}$ | $t_{DIOV}$×1.2 | – | 5 |
| Load short-circuiting detection delay time | $t_{SHORT}$ | – | $t_{SHORT}$×0.8 | $t_{SHORT}$ | $t_{SHORT}$×1.2 | – | 5 |
| Charge overcurrent detection delay time | $t_{CIOV}$ | – | $t_{CIOV}$×0.8 | $t_{CIOV}$ | $t_{CIOV}$×1.2 | – | 5 |

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

### 2. Ta = –40°C to +85°C*1

**Table 9**

(Ta = –40°C to +85°C*1 unless otherwise specified)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Test Circuit |
|---|---|---|---|---|---|---|---|
| **DETECTION VOLTAGE** | | | | | | | |
| Overcharge detection voltage | $V_{CU}$ | – | $V_{CU}$–0.045 | $V_{CU}$ | $V_{CU}$+0.030 | V | 1 |
| Overcharge release voltage | $V_{CL}$ | $V_{CL} \neq V_{CU}$ | $V_{CL}$–0.070 | $V_{CL}$ | $V_{CL}$+0.040 | V | 1 |
| | | $V_{CL} = V_{CU}$ | $V_{CL}$–0.050 | $V_{CL}$ | $V_{CL}$+0.030 | V | 1 |
| Overdischarge detection voltage | $V_{DL}$ | – | $V_{DL}$–0.070 | $V_{DL}$ | $V_{DL}$+0.045 | V | 2 |
| Overdischarge release voltage | $V_{DU}$ | $V_{DL} \neq V_{DU}$ | $V_{DU}$–0.090 | $V_{DU}$ | $V_{DU}$+0.060 | V | 2 |
| | | $V_{DL} = V_{DU}$ | $V_{DU}$–0.070 | $V_{DU}$ | $V_{DU}$+0.045 | V | 2 |
| Discharge overcurrent detection voltage | $V_{DIOV}$ | – | $V_{DIOV}$–0.010 | $V_{DIOV}$ | $V_{DIOV}$+0.010 | V | 2 |
| Load short-circuiting detection voltage | $V_{SHORT}$ | – | 0.40 | 0.50 | 0.60 | V | 2 |
| Charge overcurrent detection voltage | $V_{CIOV}$ | – | $V_{CIOV}$–0.015 | $V_{CIOV}$ | $V_{CIOV}$+0.015 | V | 2 |
| **0 V BATTERY CHARGE FUNCTION** | | | | | | | |
| 0 V battery charge starting charger voltage | $V_{0CHA}$ | 0 V battery charging function “available” | 0.0 | 0.7 | 1.5 | V | 2 |
| 0 V battery charge inhibition battery voltage | $V_{0INH}$ | 0 V battery charging function “unavailable” | 0.4 | 0.8 | 1.3 | V | 2 |
| **INTERNAL RESISTANCE** | | | | | | | |
| Resistance between VM pin and VDD pin | $R_{VMD}$ | $V_{DD}$ = 1.8 V, $V_{VM}$ = 0 V | 78 | 300 | 1310 | kΩ | 3 |
| Resistance between VM pin and VSS pin | $R_{VMS}$ | $V_{DD}$ = 3.4 V, $V_{VM}$ = 1.0 V | 7.2 | 20 | 44 | kΩ | 3 |
| **INPUT VOLTAGE** | | | | | | | |
| Operating voltage between VDD pin and VSS pin | $V_{DSOP1}$ | – | 1.5 | – | 6.5 | V | – |
| Operating voltage between VDD pin and VM pin | $V_{DSOP2}$ | – | 1.5 | – | 28 | V | – |
| **INPUT CURRENT (Product with power-down function)** | | | | | | | |
| Current consumption during operation | $I_{OPE}$ | $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 0.7 | 2.8 | 5.5 | μA | 2 |
| Current consumption at power-down | $I_{PDN}$ | $V_{DD}$ = $V_{VM}$ = 1.5 V | – | – | 0.15 | μA | 2 |
| **INPUT CURRENT (Product without power-down function)** | | | | | | | |
| Current consumption during operation | $I_{OPE}$ | $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 0.7 | 2.8 | 5.5 | μA | 2 |
| Current consumption during overdischarge | $I_{OPED}$ | $V_{DD}$ = $V_{VM}$ = 1.5 V | – | – | 3.8 | μA | 2 |
| **OUTPUT RESISTANCE** | | | | | | | |
| CO pin resistance “H” | $R_{COH}$ | $V_{CO}$ = 3.0 V, $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 2.4 | 10 | 30 | kΩ | 4 |
| CO pin resistance “L” | $R_{COL}$ | $V_{CO}$ = 0.4 V, $V_{DD}$ = 4.6 V, $V_{VM}$ = 0 V | 2.4 | 10 | 30 | kΩ | 4 |
| DO pin resistance “H” | $R_{DOH}$ | $V_{DO}$ = 3.0 V, $V_{DD}$ = 3.4 V, $V_{VM}$ = 0 V | 2.4 | 10 | 30 | kΩ | 4 |
| DO pin resistance “L” | $R_{DOL}$ | $V_{DO}$ = 0.4 V, $V_{DD}$ = 1.8 V, $V_{VM}$ = 0 V | 2.4 | 10 | 30 | kΩ | 4 |
| **DELAY TIME** | | | | | | | |
| Overcharge detection delay time | $t_{CU}$ | – | $t_{CU}$×0.6 | $t_{CU}$ | $t_{CU}$×1.6 | – | 5 |
| Overdischarge detection delay time | $t_{DL}$ | – | $t_{DL}$×0.6 | $t_{DL}$ | $t_{DL}$×1.6 | – | 5 |
| Discharge overcurrent detection delay time | $t_{DIOV}$ | – | $t_{DIOV}$×0.6 | $t_{DIOV}$ | $t_{DIOV}$×1.6 | – | 5 |
| Load short-circuiting detection delay time | $t_{SHORT}$ | – | $t_{SHORT}$×0.6 | $t_{SHORT}$ | $t_{SHORT}$×1.6 | – | 5 |
| Charge overcurrent detection delay time | $t_{CIOV}$ | – | $t_{CIOV}$×0.6 | $t_{CIOV}$ | $t_{CIOV}$×1.6 | – | 5 |

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

## ■ Test Circuits

**Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin ($V_{CO}$) and DO pin ($V_{DO}$) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to $V_{VM}$ and the DO pin level with respect to $V_{SS}$.**

### 1. Overcharge Detection Voltage, Overcharge Release Voltage (Test Circuit 1)

Overcharge detection voltage ($V_{CU}$) is defined as the voltage V1 at which $V_{CO}$ goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V, V2 = 0 V. Overcharge release voltage ($V_{CL}$) is defined as the voltage V1 at which $V_{CO}$ goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage ($V_{HC}$) is defined as the difference between $V_{CU}$ and $V_{CL}$.

### 2. Overdischarge Detection Voltage, Overdischarge Release Voltage (Test Circuit 2)

Overdischarge detection voltage ($V_{DL}$) is defined as the voltage V1 at which $V_{DO}$ goes from "H" to "L" when the voltage V1 is gradually decreased from the starting condition of V1 = 3.4 V, V2 = 0 V. Overdischarge release voltage ($V_{DU}$) is defined as the voltage V1 at which $V_{DO}$ goes from "L" to "H" when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage ($V_{HD}$) is defined as the difference between $V_{DU}$ and $V_{DL}$.

### 3. Discharge Overcurrent Detection Voltage (Test Circuit 2)

Discharge overcurrent detection voltage ($V_{DIOV}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "H" to "L" is discharge overcurrent delay time ($t_{DIOV}$) when the voltage V2 is increased from the starting condition of V1 = 3.4 V, V2 = 0 V.

### 4. Load Short-circuiting Detection Voltage (Test Circuit 2)

Load short-circuiting detection voltage ($V_{SHORT}$) is defined as the voltage V2 whose delay time for changing $V_{DO}$ from "H" to "L" is load short-circuiting delay time ($t_{SHORT}$) when the voltage V2 is increased from the starting condition of V1 = 3.4 V, V2 = 0 V.

### 5. Charge Overcurrent Detection Voltage (Test Circuit 2)

Charge overcurrent detection voltage ($V_{CIOV}$) is defined as the voltage V2 whose delay time for changing $V_{CO}$ from "H" to "L" is charge overcurrent delay time ($t_{CIOV}$) when the voltage V2 is decreased from the starting condition of V1 = 3.4 V, V2 = 0 V.

### 6. Operating Current Consumption (Test Circuit 2)

The operating current consumption ($I_{OPE}$) is the current that flows through the VDD pin ($I_{DD}$) under the set conditions of V1 = 3.4 V and V2 = 0 V.

### 7. Power-down Current Consumption, Current consumption during overdischarge (Test Circuit 2)

**Product with power-down function**

The power-down current consumption ($I_{PDN}$) is $I_{DD}$ under the set conditions of V1 = V2 = 1.5 V.

**Product without power-down function**

The overdischarge current consumption ($I_{OPED}$) is $I_{DD}$ under the set conditions of V1 = V2 = 1.5 V.

### 8. Resistance between VM Pin and VDD Pin (Test Circuit 3)

$R_{VMD}$ is the resistance between VM pin and VDD pin under the set conditions of V1 = 1.8 V, V2 = 0 V.

### 9. Resistance between VM Pin and VSS Pin (Test Circuit 3)

$R_{VMS}$ is the resistance between VM pin and VSS pin under the set conditions of V1 = 3.4 V, V2 = 1.0 V.

### 10. CO Pin Resistance "H" (Test Circuit 4)

The CO pin resistance "H" ($R_{COH}$) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V3 = 3.0 V.

### 11. CO Pin Resistance "L" (Test Circuit 4)

The CO pin resistance "L" ($R_{COL}$) is the resistance between VM pin and CO pin under the set conditions of V1 = 4.6 V, V2 = 0 V, V3 = 0.4 V.

### 12. DO Pin Resistance "H" (Test Circuit 4)

The DO pin H resistance ($R_{DOH}$) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V4 = 3.0 V.

### 13. DO Pin Resistance "L" (Test Circuit 4)

The DO pin L resistance ($R_{DOL}$) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V2 = 0 V, V4 = 0.4 V.

### 14. Overcharge Detection Delay Time (Test Circuit 5)

The overcharge detection delay time ($t_{CU}$) is the time needed for $V_{CO}$ to go to "L" just after the voltage V1 increases and exceeds $V_{CU}$ under the set condition of V1 = 3.4 V, V2 = 0 V.

### 15. Overdischarge Detection Delay Time (Test Circuit 5)

The overdischarge detection delay time ($t_{DL}$) is the time needed for $V_{DO}$ to go to "L" after the voltage V1 decreases and falls below $V_{DL}$ under the set condition of V1 = 3.4 V, V2 = 0 V.

### 16. Discharge Overcurrent Detection Delay Time (Test Circuit 5)

The discharge overcurrent detection delay time ($t_{DIOV}$) is the time needed for $V_{DO}$ to go to "L" after the voltage V2 increases and exceeds $V_{DIOV}$ under the set conditions of V1 = 3.4 V, V2 = 0 V.

### 17. Load Short-circuiting Detection Delay Time (Test Circuit 5)

The load short-circuiting detection delay time ($t_{SHORT}$) is the time needed for $V_{DO}$ to go to "L" after the voltage V2 increases and exceeds $V_{SHORT}$ under the set conditions of V1 = 3.4 V, V2 = 0 V.

### 18. Charge Overcurrent Detection Delay Time (Test Circuit 5)

The charge overcurrent detection delay time ($t_{CIOV}$) is the time needed for $V_{CO}$ to go to "L" after the voltage V2 decreases and falls below $V_{CIOV}$ under the set condition of V1 = 3.4 V, V2 = 0 V.

### 19. 0 V Battery Charge Starting Charger Voltage (Products with 0 V Battery Charging Function Is "Available") (Test Circuit 2)

The 0 V charge starting charger voltage ($V_{0CHA}$) is defined as the voltage V2 at which $V_{CO}$ goes to "H" ($V_{CO} = V_{DD}$) when the voltage V2 is gradually decreased from the starting condition of V1 = V2 = 0 V.

### 20. 0 V Battery Charge Inhibition Battery Voltage (Products with 0 V Battery Charging Function Is "Unavailable") (Test Circuit 2)

The 0 V charge inhibition battery voltage ($V_{0INH}$) is defined as the voltage V1 at which $V_{CO}$ goes to "L" ($V_{VM}$ +0.1 V or lower) when the voltage V1 is gradually decreased, after setting V1 = 1.5 V, V2 = –4.0 V.

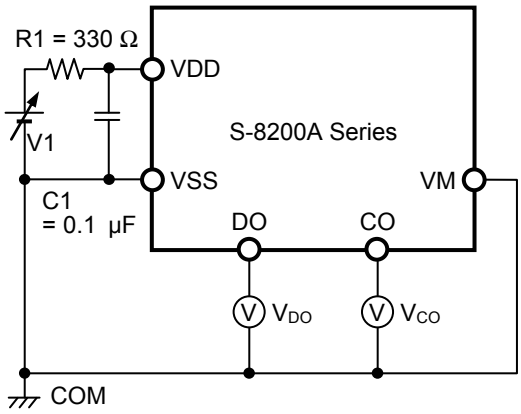



**Figure 5 Test Circuit 1**

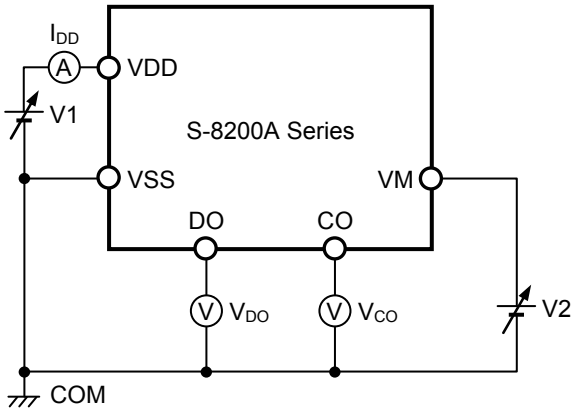



**Figure 6 Test Circuit 2**

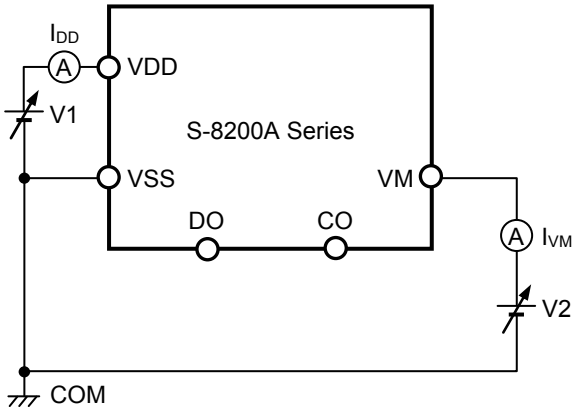



**Figure 7 Test Circuit 3**

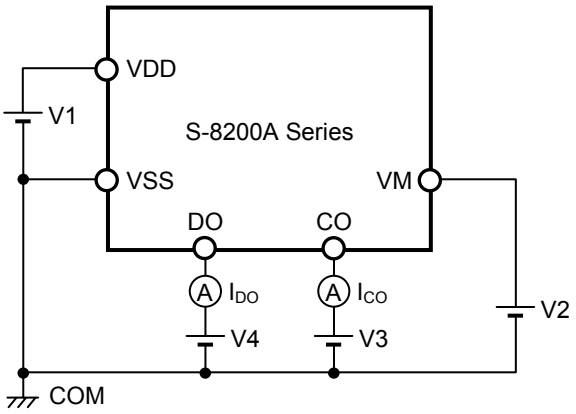



**Figure 8 Test Circuit 4**

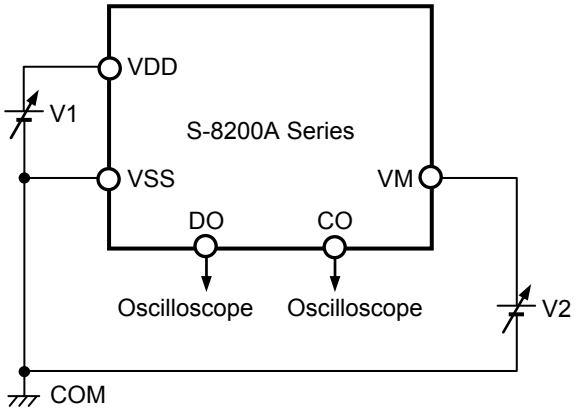



**Figure 9 Test Circuit 5**

## ■ Operation

**Remark** Refer to the "■ **Battery Protection IC Connection Example**".

### 1. Normal Status

The S-8200A Series monitors the voltage of the battery connected between the VDD pin and VSS pin and the voltage difference between the VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage ($V_{DL}$) to overcharge detection voltage ($V_{CU}$), and the VM pin voltage is in the range from the charge overcurrent detection voltage ($V_{CIOV}$) to discharge overcurrent detection voltage ($V_{DIOV}$), the IC turns both the charging and discharging control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.
The resistance ($R_{VMD}$) between the VM pin and VDD pin, and the resistance ($R_{VMS}$) between the VM pin and VSS pin are not connected in the normal status.

**Caution When the battery is connected for the first time, discharging may not be enabled. In this case,**
**Short the VM pin and VSS pin, or**
**Set the VM pin's voltage at the level of $V_{CIOV}$ or more and $V_{DIOV}$ or less by connecting the charger**
**The IC returns to the normal status.**

### 2. Overcharge Status

When the battery voltage becomes higher than $V_{CU}$ during charging in the normal status and detection continues for the overcharge detection delay time ($t_{CU}$) or longer, the S-8200A Series turns the charging control FET off to stop charging. This condition is called the overcharge status.
$R_{VMD}$ and $R_{VMS}$ are not connected in the overcharge status.
The overcharge status is released in the following two cases.

(1) In the case that the VM pin voltage is lower than $V_{DIOV}$, the S-8200A Series releases the overcharge status when the battery voltage falls below $V_{CL}$.
(2) In the case that the VM pin voltage is higher than or equal to $V_{DIOV}$, the S-8200A Series releases the overcharge status when the battery voltage falls below $V_{CU}$.

The discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises more than the voltage at VSS pin due to the $V_f$ voltage of the parasitic diode, because the discharge current flows through the parasitic diode in the charging control FET. If this VM pin voltage is higher than or equal to $V_{DIOV}$, the S-8200A Series releases the overcharge status when the battery voltage is lower than or equal to $V_{CU}$.

**Caution If the battery is charged to a voltage higher than $V_{CU}$ and the battery voltage does not fall below $V_{CU}$ even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below $V_{CU}$. Since an actual battery has an internal impedance of tens of mΩ, the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.**

### 3. Overdischarge Status

When the battery voltage falls below overdischarge detection voltage ($V_{DL}$) during discharging in the normal status and the detection continues for the overdischarge detection delay time ($t_{DL}$) or longer, the S-8200A Series turns the discharging control FET off to stop discharging. This condition is called the overdischarge status.
Under the overdischarge status, the VM pin and VDD pin are shorted by $R_{VMD}$ in the IC. The VM pin voltage is pulled up by $R_{VMD}$.
When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than typ. −0.7 V, the S-8200A Series releases the overdischarge status when the battery voltage reaches $V_{DL}$ or higher.
When VM pin voltage is not lower than typ. −0.7 V, the S-8200A Series releases the overdischarge status when the battery voltage reaches $V_{DU}$ or higher.
$R_{VMS}$ is not connected in the overdischarge status.

**With power-down function**
Under the overdischarge status, when voltage difference between the VM pin and VDD pin is 0.8 V (typ.) or lower, the current consumption is reduced to the power-down current consumption ($I_{PDN}$).

### 4. Discharge Overcurrent Status (Discharge Overcurrent, Load Short-circuiting)

When a battery in the normal status is in the status where the voltage of the VM pin is equal to or higher than $V_{DIOV}$ because the discharge current is higher than the specified value and the status lasts for the discharge overcurrent detection delay time ($t_{DIOV}$), the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.
In the discharge overcurrent status, the VM pin and VSS pin are shorted by the $R_{VMS}$ in the IC. However, the voltage of the VM pin is at the $V_{DD}$ potential due to the load as long as the load is connected. When the load is disconnected, the VM pin returns to the $V_{SS}$ potential.
The voltage at the VM pin returns to $V_{DIOV}$ or lower, the S-8200A Series releases the discharge overcurrent status.
$R_{VMD}$ is not connected in the discharge overcurrent detection status.

### 5. Charge Overcurrent Status

When a battery in the normal status is in the status where the voltage of the VM pin is lower than $V_{CIOV}$ because the charge current is higher than the specified value and the status lasts for the charge overcurrent detection delay time ($t_{CIOV}$), the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.
The S-8200A Series releases the charge overcurrent status when, the voltage at the VM pin returns to $V_{CIOV}$ or higher by removing the charger.
The charge overcurrent detection function does not work in the overdischarge status.
$R_{VMD}$ and $R_{VMS}$ are not connected in the charge overcurrent status.

## 6. 0 V Battery Charging Function "Available"

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage ($V_{0CHA}$) or a higher voltage is applied between the EB+ and EB− pins by connecting a charger, the charging control FET gate is fixed to the $V_{DD}$ potential.
When the voltage between the gate and source of the charging control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charging control FET is turned on to start charging. At this time, the discharging control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than $V_{DU}$, the S-8200A Series enters the normal status.

**Caution 1. Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charging function.**
**2. The 0 V battery charge function has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charging function is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than $V_{DL}$.**

## 7. 0 V Battery Charging Function "Unavailable"

This function inhibits recharging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage ($V_{0INH}$) or lower, the charging control FET gate is fixed to the EB− pin voltage to inhibit charging. When the battery voltage is $V_{0INH}$ or higher, charging can be performed.

**Caution Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charging function.**

## 8. Delay Circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

**Remark** $t_{DIOV}$ and $t_{SHORT}$ start when $V_{DIOV}$ is detected. When $V_{SHORT}$ is detected over $t_{SHORT}$ after $V_{DIOV}$, the S-8200A turns the discharging control FET off within $t_{SHORT}$ from the time of detecting $V_{SHORT}$.

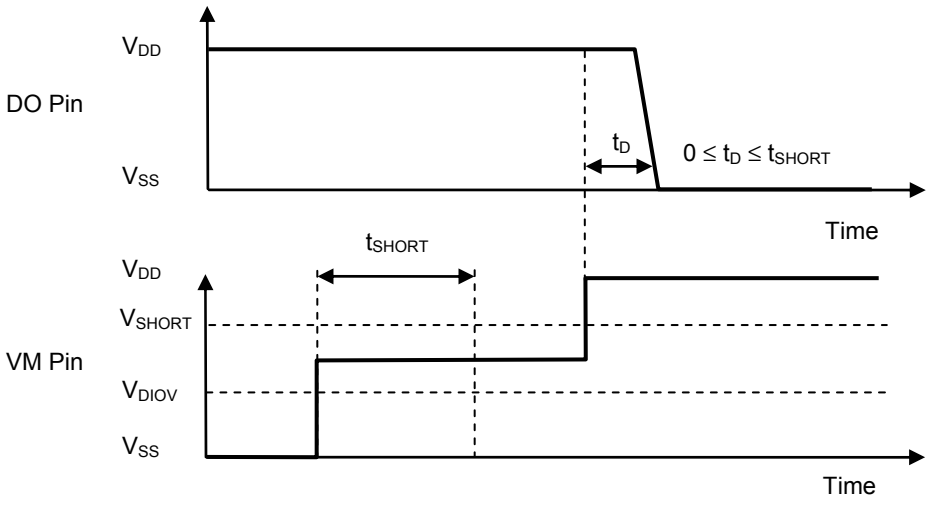
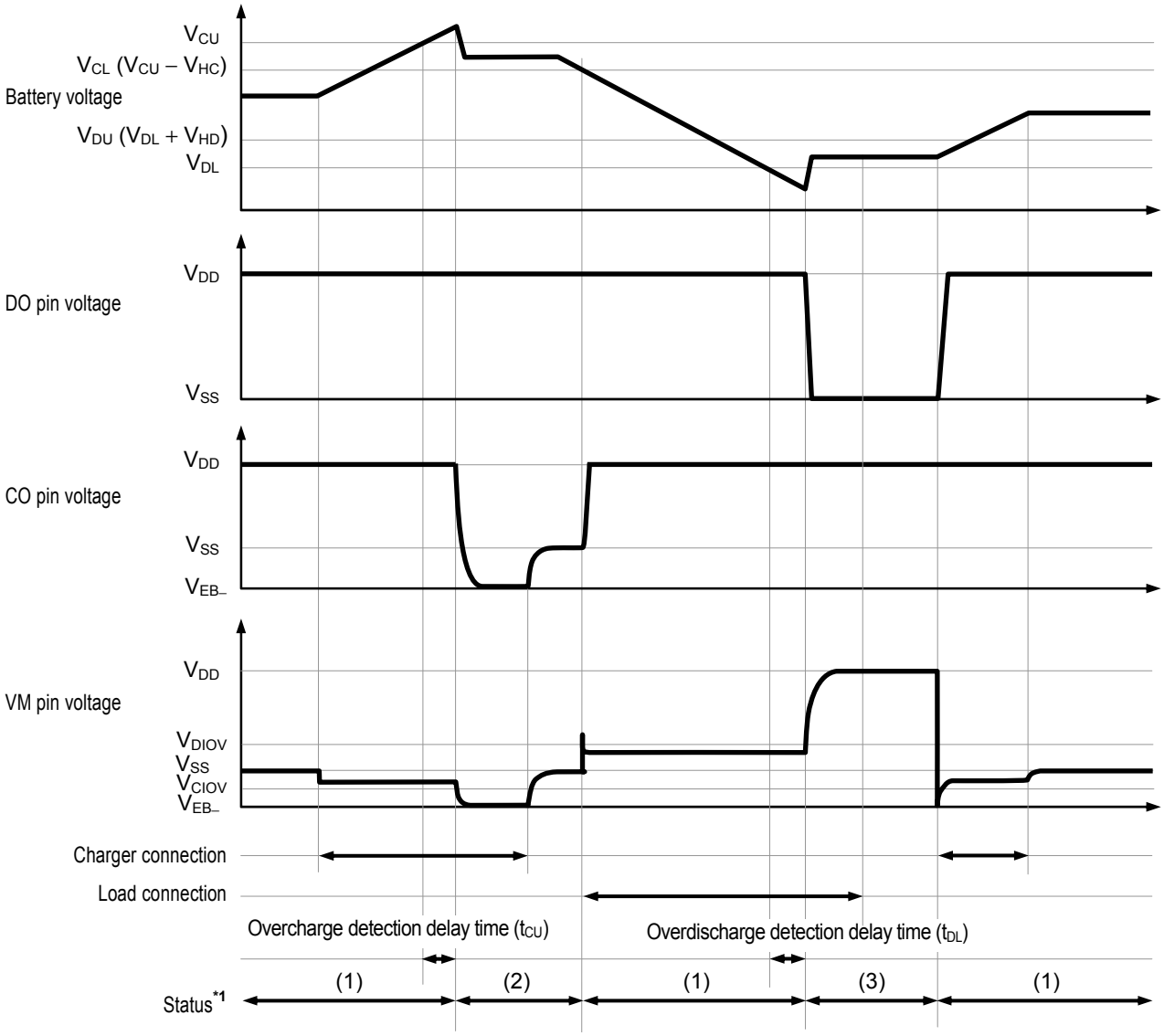



**Figure 10**

## ■ Timing Chart

### 1. Overcharge Detection, Overdischarge Detection

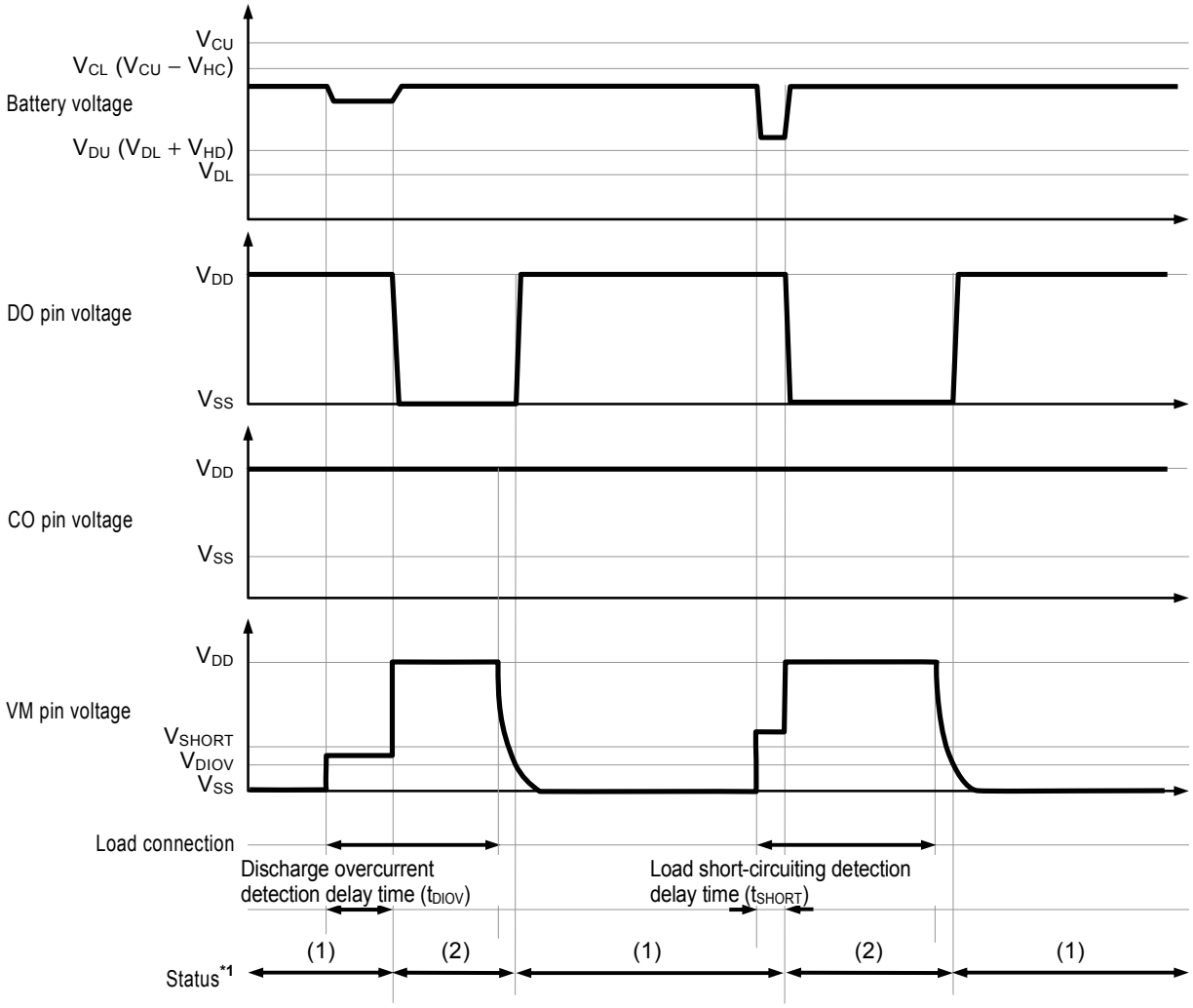



***1.** (1) : Normal status
(2) : Overcharge status
(3) : Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

**Figure 11**

**2. Discharge Overcurrent Detection**

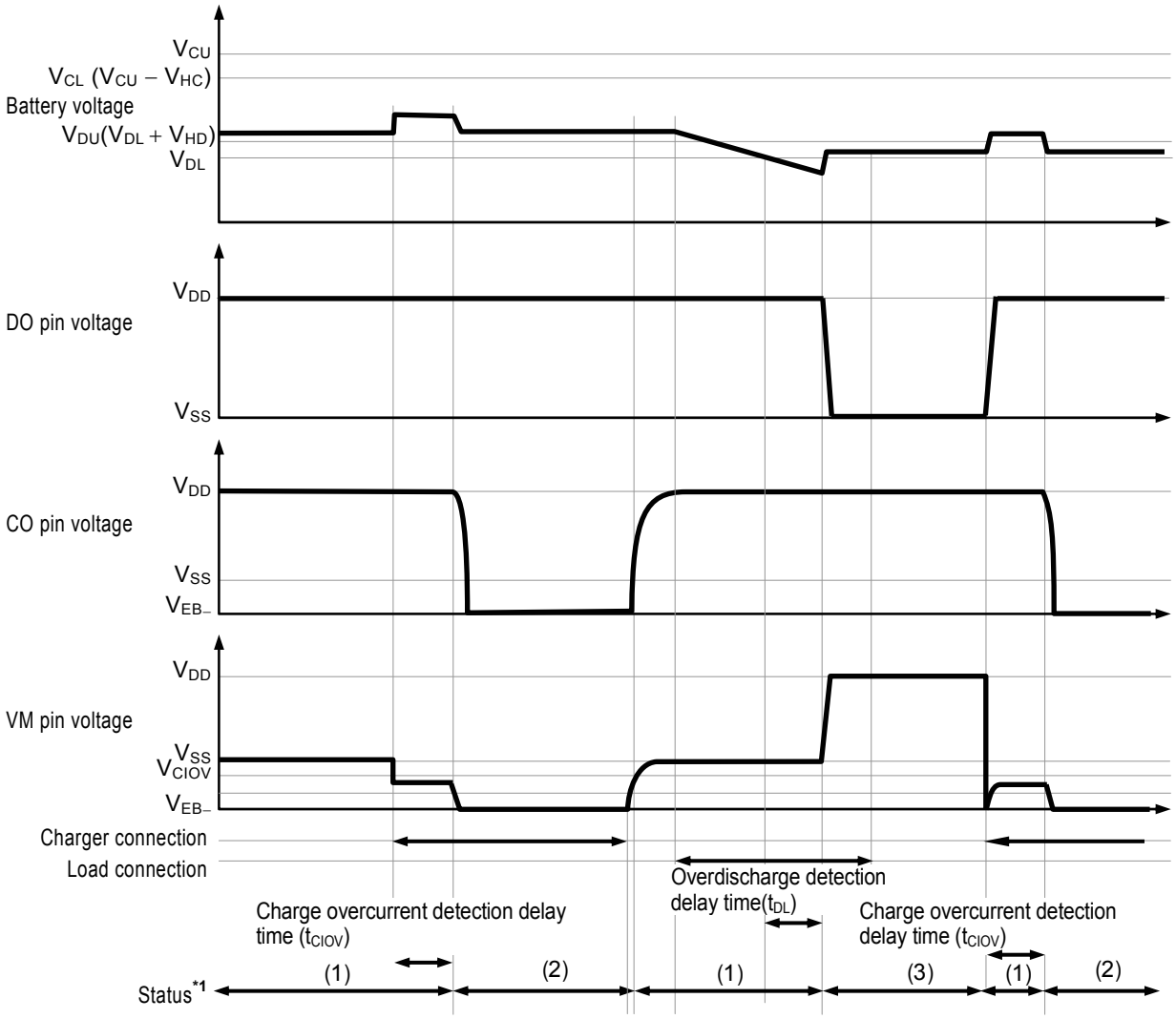



***1.** (1) : Normal status
(2) : Discharge overcurrent status

**Remark** The charger is assumed to charge with a constant current.

**Figure 12**

### 3. Charge Overcurrent Detection




***1.** (1) : Normal status
(2) : Charge overcurrent status
(3) : Overdischarge status

**Remark** The charger is assumed to charge with a constant current.

**Figure 13**

## ■ Battery Protection IC Connection Example

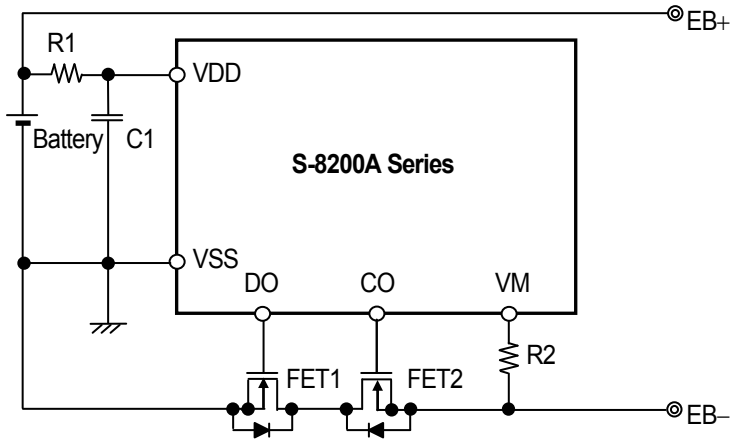



**Figure 14**

**Table 10 Constants for External Components**

| Symbol | Part | Purpose | Typ. | Min. | Max. | Remark |
|---|---|---|---|---|---|---|
| FET1 | N-channel MOS FET | Discharge control | – | – | – | Threshold voltage ≤ Overdischarge detection voltage *1<br>Gate to source withstanding voltage ≥ Charger voltage *2 |
| FET2 | N-channel MOS FET | Charge control | – | – | – | Threshold voltage ≤ Overdischarge detection voltage *1<br>Gate to source withstanding voltage ≥ Charger voltage *2 |
| R1 | Resistor | ESD protection,<br>For power fluctuation | 330 Ω | 150 Ω | 1 kΩ | Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption. *3 |
| C1 | Capacitor | For power fluctuation | 0.1 μF | 0.068 μF | 1.0 μF | Connect a capacitor of 0.068 μF or higher between VDD pin and VSS pin. *4 |
| R2 | Resistor | Protection for reverse connection of a charger | 2 kΩ | 300 Ω | 4 kΩ | Select as large a resistance as possible to prevent current when a charger is connected in reverse. *5 |

***1.** If the threshold voltage of an FET is low, the FET may not cut the charging current. If an FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

***2.** If the withstanding voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

***3.** An accuracy of overcharge detection voltage is guaranteed by R1 = 330 Ω. Connecting resistors with other values worsen the accuracy. In case of connecting larger resistor to R1, the voltage between the VDD pin and VSS pin may exceed the absolute maximum rating because the current flows to the IC from the charger due to reverse connection of charger. Connect a resistor of 150 Ω or more to R1 for ESD protection.

***4.** When connecting a resistor of 150 Ω or less to R1 or a capacitor of 0.068 μF or less to C1, the IC may malfunction when power dissipation is largely fluctuated.

***5.** When a resistor more than 4 kΩ is connected to R2, the charge current may not be cut.

**Caution 1. The above constants may be changed without notice.**

**2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.**

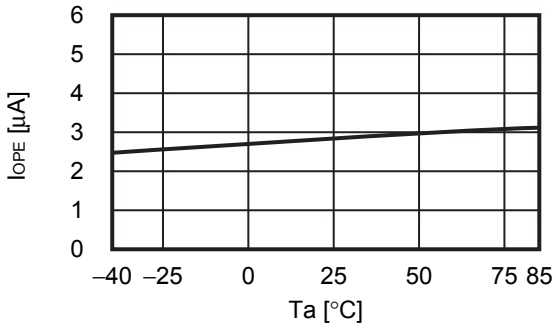
## ■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- SII claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

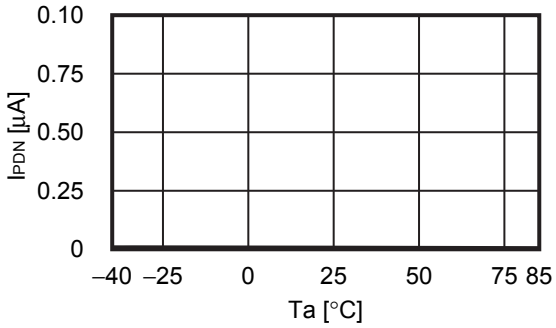
## ■ Characteristics (Typical Data)

### 1. Current Consumption

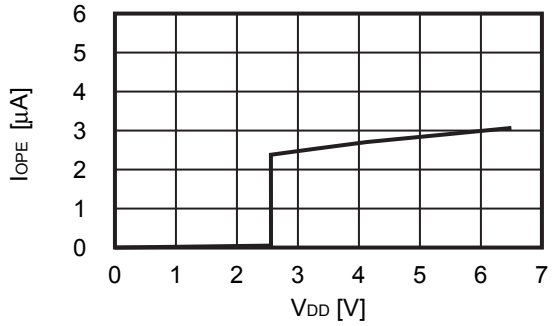
#### 1. 1 $I_{OPE}$ vs. Ta




#### 1. 2 $I_{PDN}$ vs. Ta

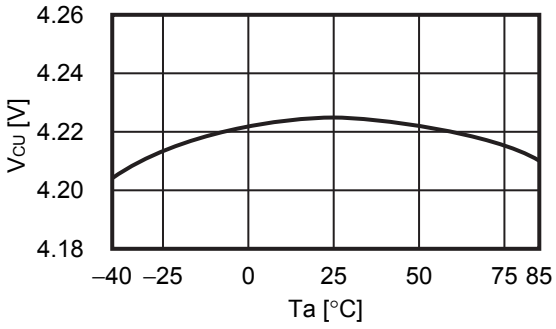



#### 1. 3 $I_{OPE}$ vs. $V_{DD}$

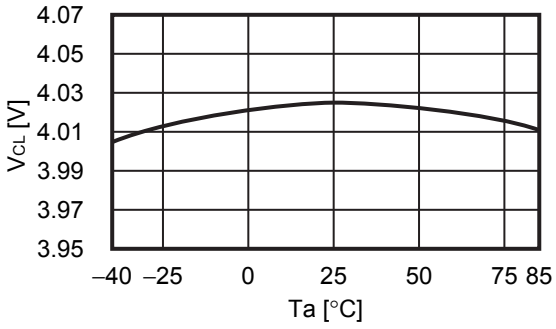


## 2. Overcharge Detection / Release Voltage, Overdischarge Detection / Release Voltage, Overcurrent Detection Voltage, Charge Overcurrent Detection Voltage, and Delay Time

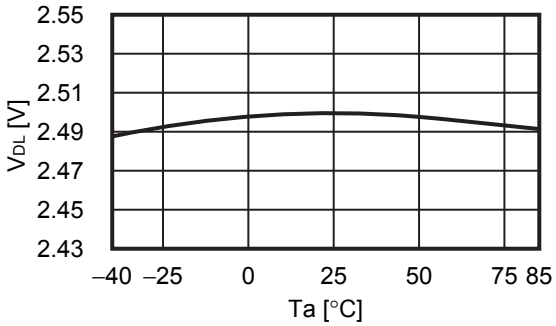
### 2. 1 $V_{CU}$ vs. Ta



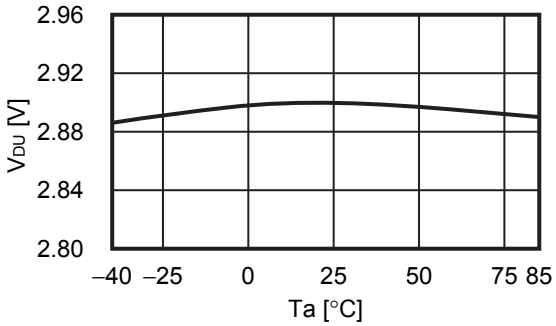

### 2. 2 $V_{CL}$ vs. Ta



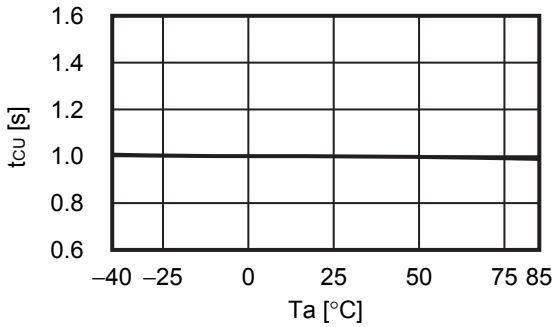

### 2. 3 $V_{DL}$ vs. Ta



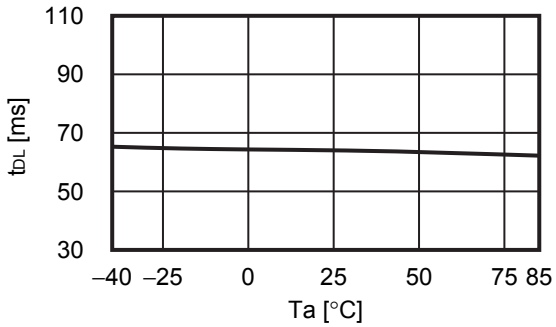

### 2. 4 $V_{DU}$ vs. Ta



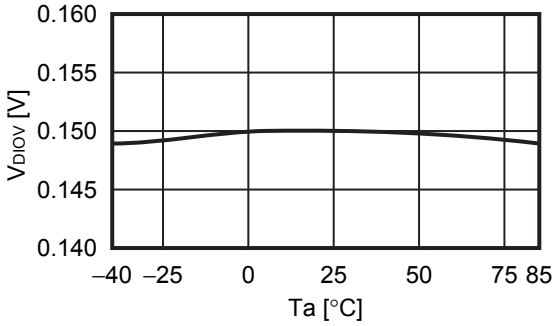

### 2. 5 $t_{CU}$ vs. Ta



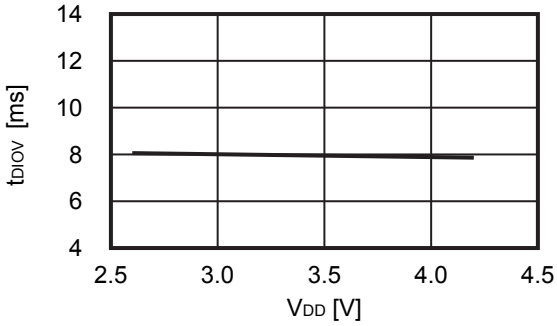

### 2. 6 $t_{DL}$ vs. Ta



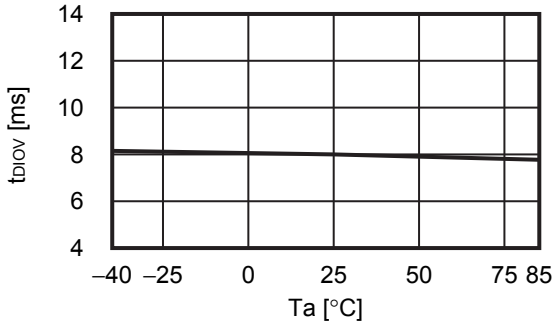

### 2. 7 $V_{DIOV}$ vs. Ta



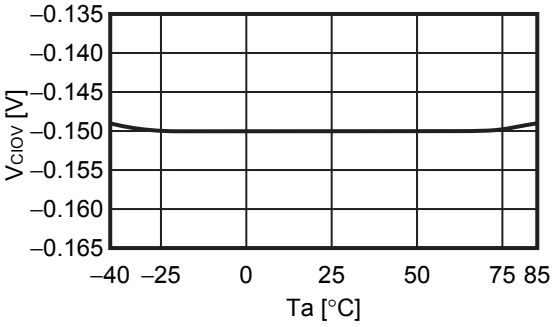

### 2. 8 $t_{DIOV}$ vs. $V_{DD}$



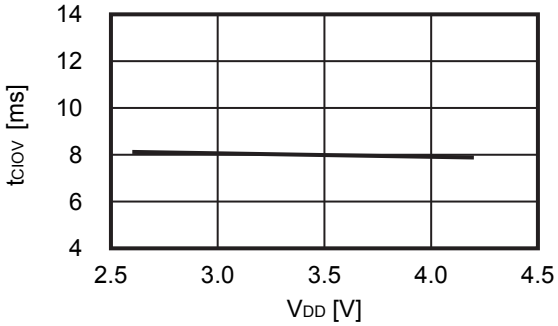
**2. 9 $t_{DIOV}$ vs. Ta**



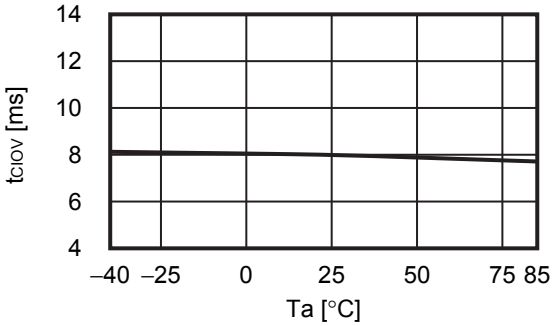

**2. 10 $V_{CIOV}$ vs. Ta**



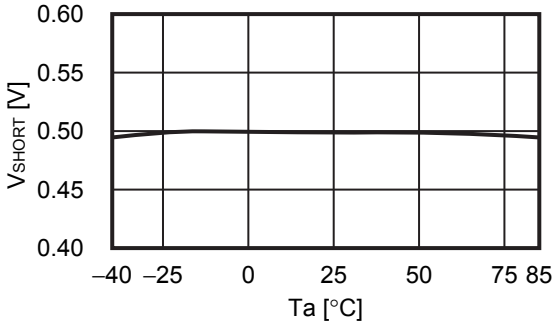

**2. 11 $t_{CIOV}$ vs. $V_{DD}$**



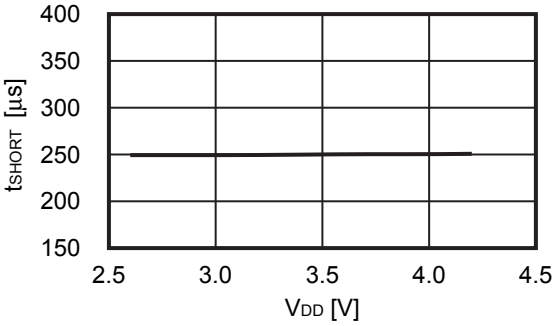

**2. 12 $t_{CIOV}$ vs. Ta**



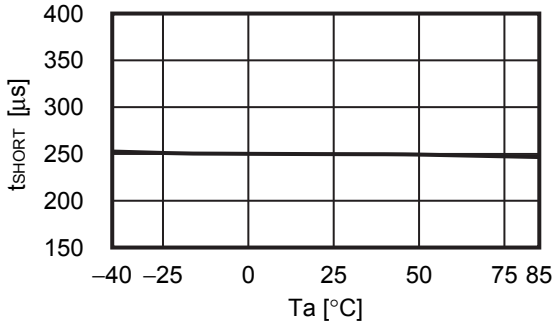

**2. 13 $V_{SHORT}$ vs. Ta**




**2. 14 $t_{SHORT}$ vs. $V_{DD}$**

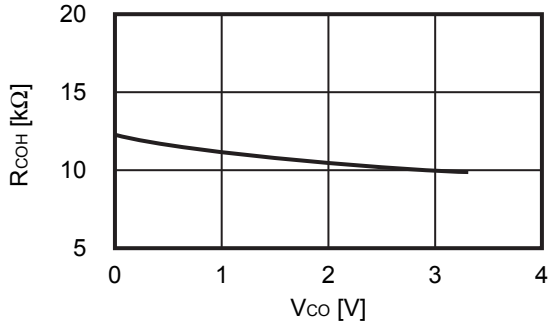



**2. 15 $t_{SHORT}$ vs. Ta**

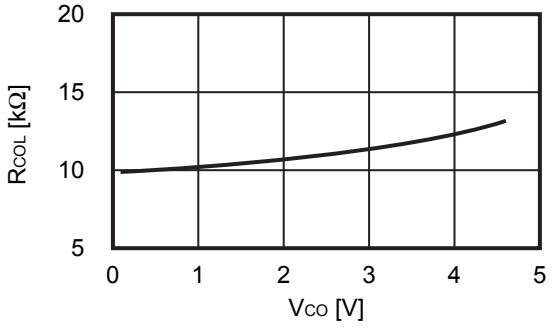


## 3. CO pin / DO pin

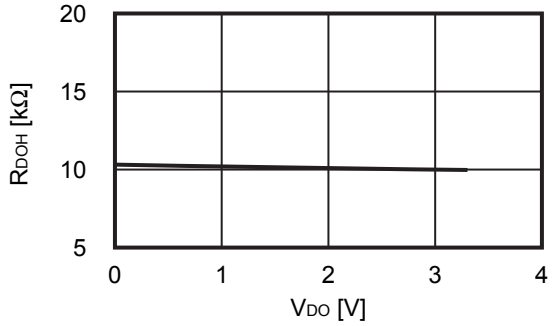
### 3. 1 $R_{COH}$ vs. $V_{CO}$



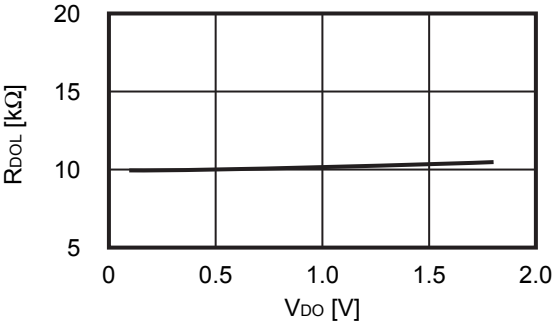

### 3. 2 $R_{COL}$ vs. $V_{CO}$




### 3. 3 $R_{DOH}$ vs. $V_{DO}$



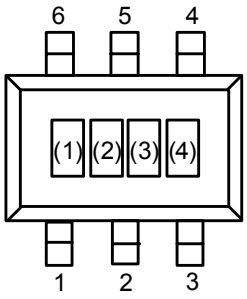

### 3. 4 $R_{DOL}$ vs. $V_{DO}$



## ■ Marking Specifications

### 1. SOT-23-6

SOT-23-6
Top view




(1) to (3): Product Code (refer to **Product Name vs. Product Code**)
(4): Lot number

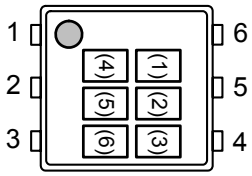
**Product Name vs. Product Code**

| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-8200AAC-M6T1U | V | 3 | C |

**Remark** Please contact our sales office for the products other than those specified above.

### 2. SNT-6A

SNT-6A
Top view

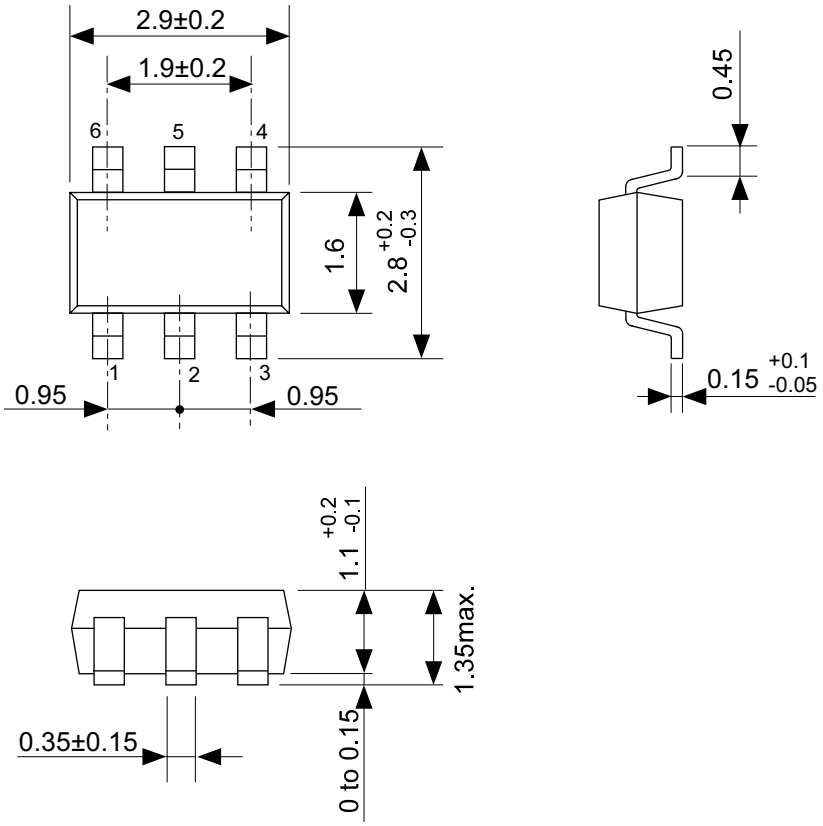



(1) to (3): Product Code (refer to **Product Name vs. Product Code**)
(4) to (6): Lot number

**Product Name vs. Product Code**

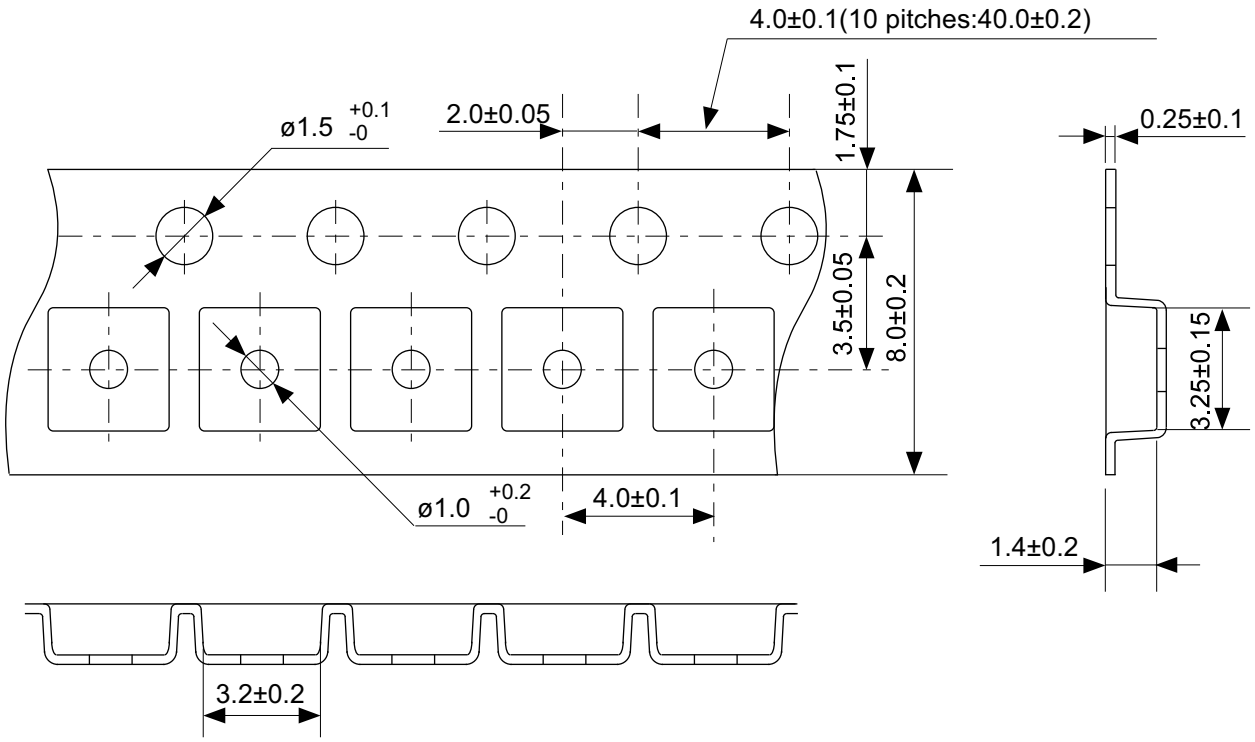
| Product Name | Product Code | | |
|---|---|---|---|
| | (1) | (2) | (3) |
| S-8200AAA-I6T1U | V | 3 | A |
| S-8200AAB-I6T1U | V | 3 | B |
| S-8200AAC-I6T1U | V | 3 | C |
| S-8200AAD-I6T1U | V | 3 | D |
| S-8200AAF-I6T1U | V | 3 | F |

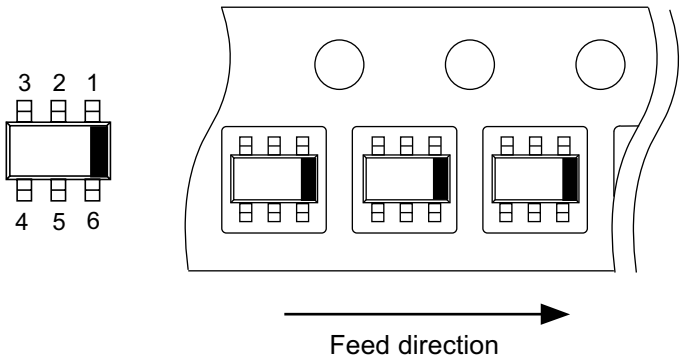
**Remark** Please contact our sales office for the products other than those specified above.




No. MP006-A-P-SD-2.0

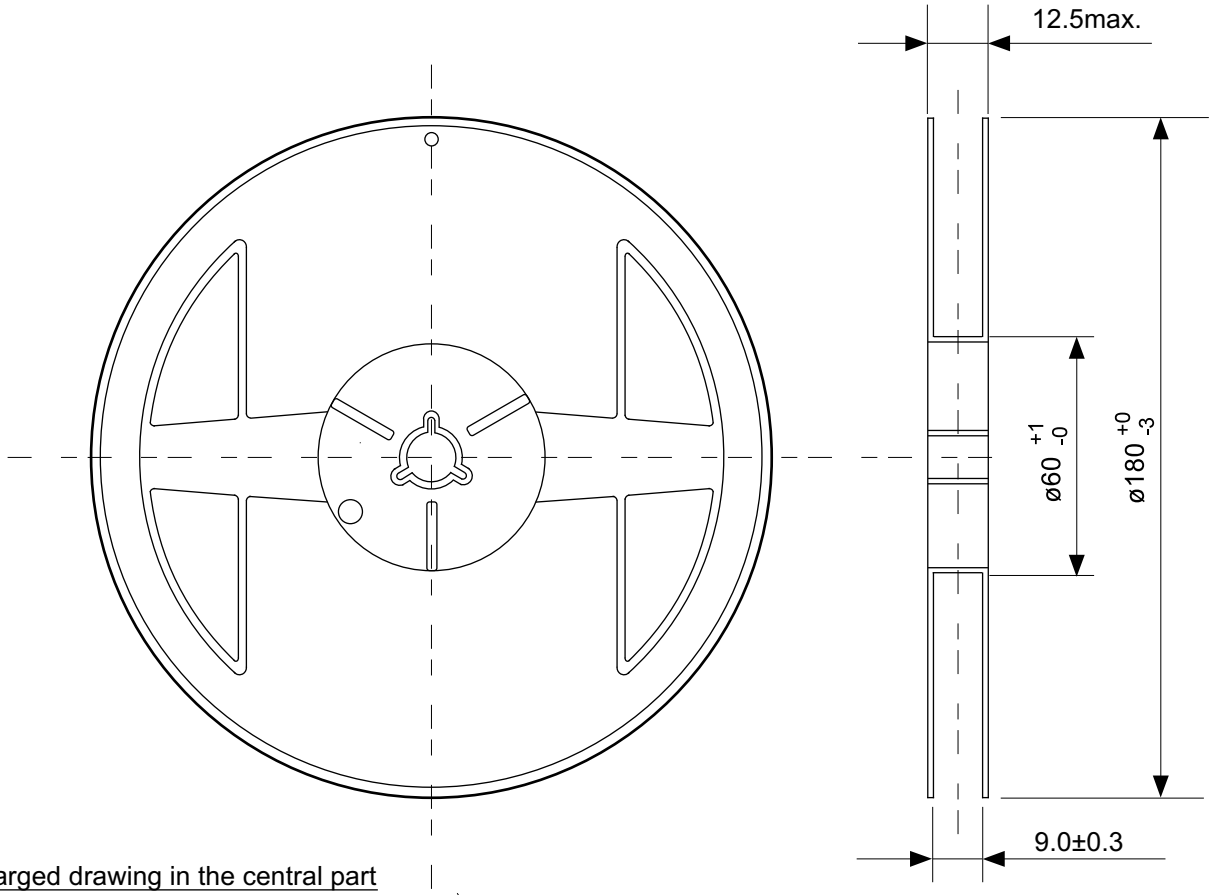
| | |
|---|---|
| TITLE | SOT236-A-PKG Dimensions |
| No. | MP006-A-P-SD-2.0 |
| SCALE | |
| UNIT | mm |
| | |
| Seiko Instruments Inc. | |



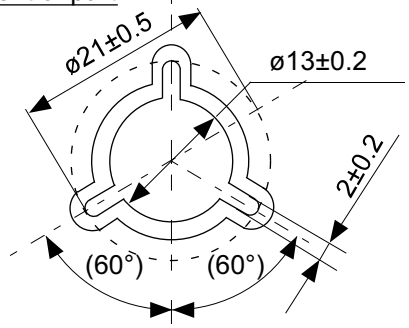




No. MP006-A-C-SD-3.1

| | |
|---|---|
| TITLE | SOT236-A-Carrier Tape |
| No. | MP006-A-C-SD-3.1 |
| SCALE | |
| UNIT | mm |
| | |
| Seiko Instruments Inc. | |

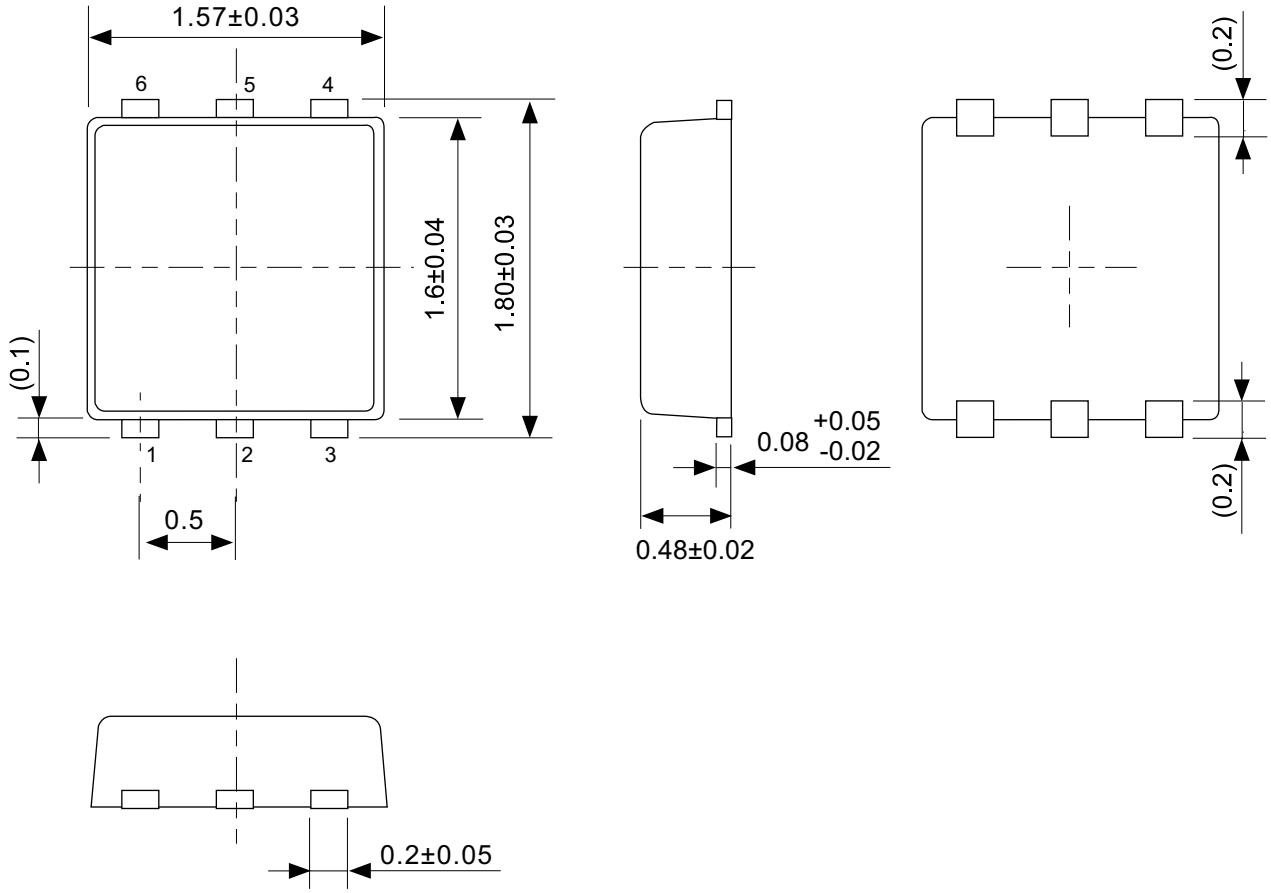



Enlarged drawing in the central part



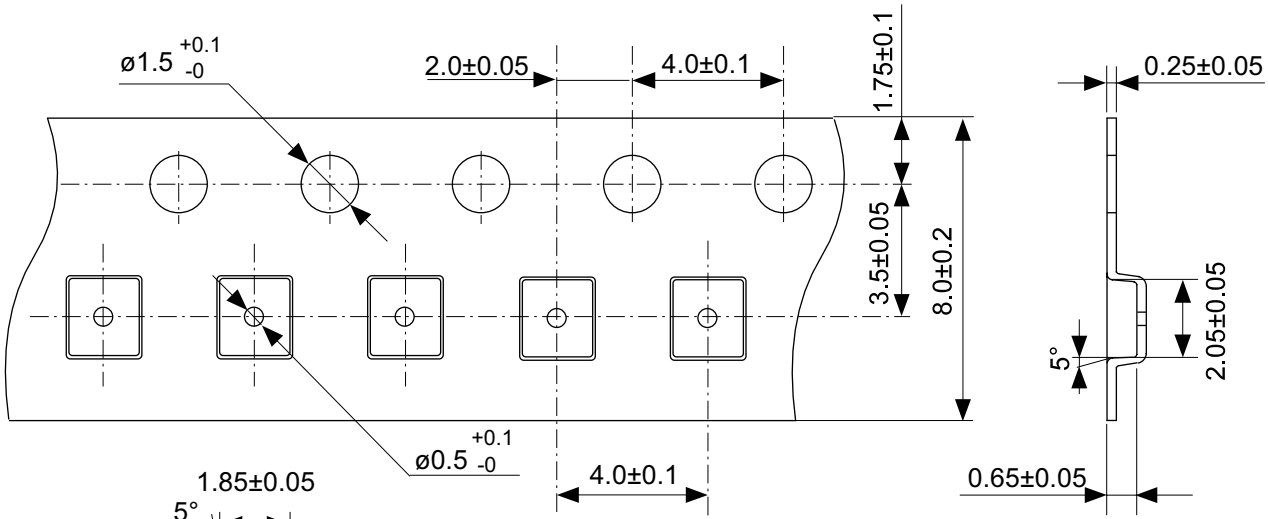

No. MP006-A-R-SD-2.1

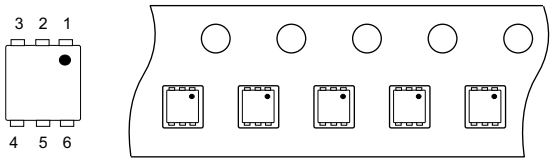
| | | | |
|---|---|---|---|
| TITLE | SOT236-A-Reel | | |
| No. | MP006-A-R-SD-2.1 | | |
| SCALE | | QTY | 3,000 |
| UNIT | mm | | |
| | | | |
| Seiko Instruments Inc. | | | |




No. PG006-A-P-SD-2.0

| | |
|---|---|
| TITLE | SNT-6A-A-PKG Dimensions |
| No. | PG006-A-P-SD-2.0 |
| SCALE | |
| UNIT | mm |
| | |
| Seiko Instruments Inc. | |

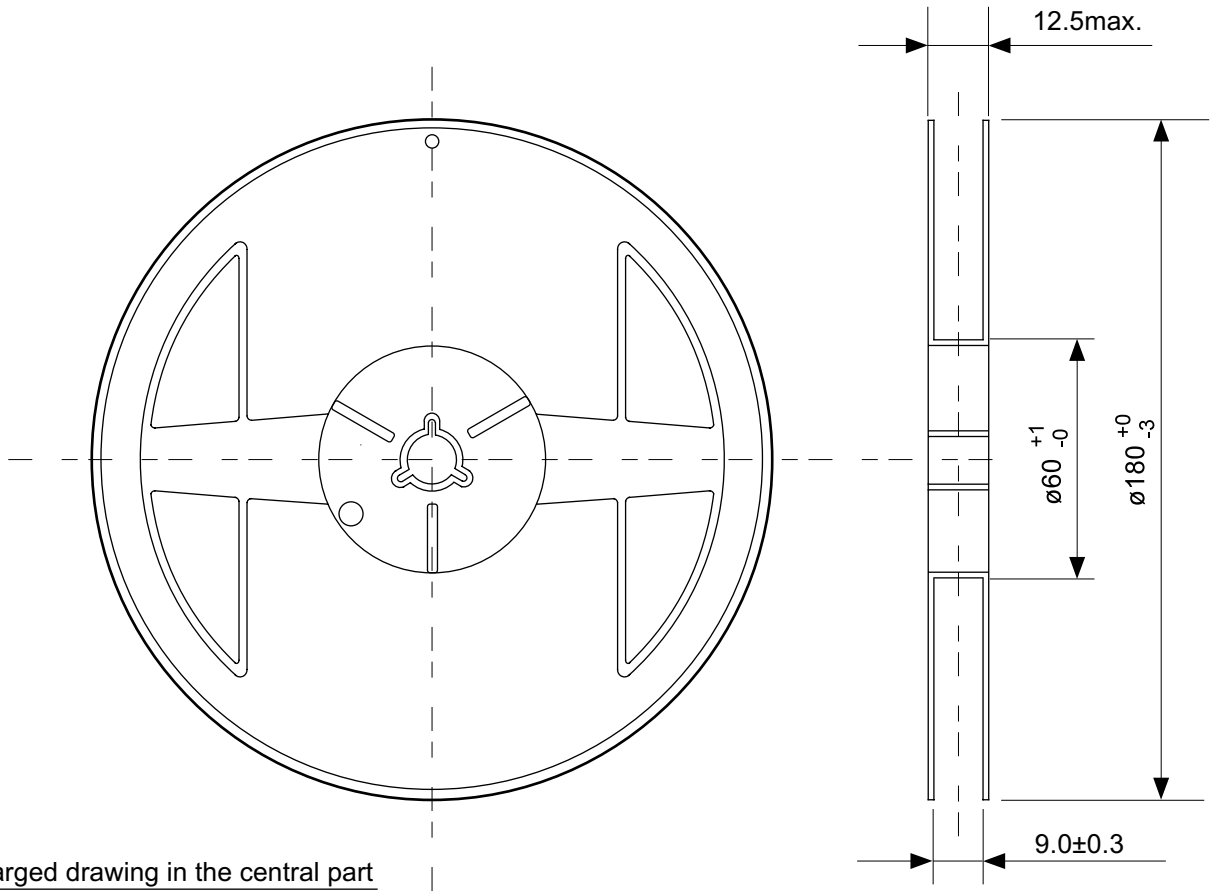


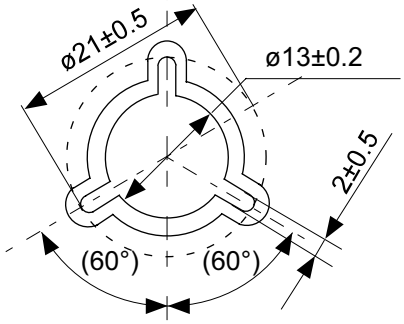

Feed direction

No. PG006-A-C-SD-1.0

| | |
|---|---|
| TITLE | SNT-6A-A-Carrier Tape |
| No. | PG006-A-C-SD-1.0 |
| SCALE | |
| UNIT | mm |
| | |
| Seiko Instruments Inc. | |

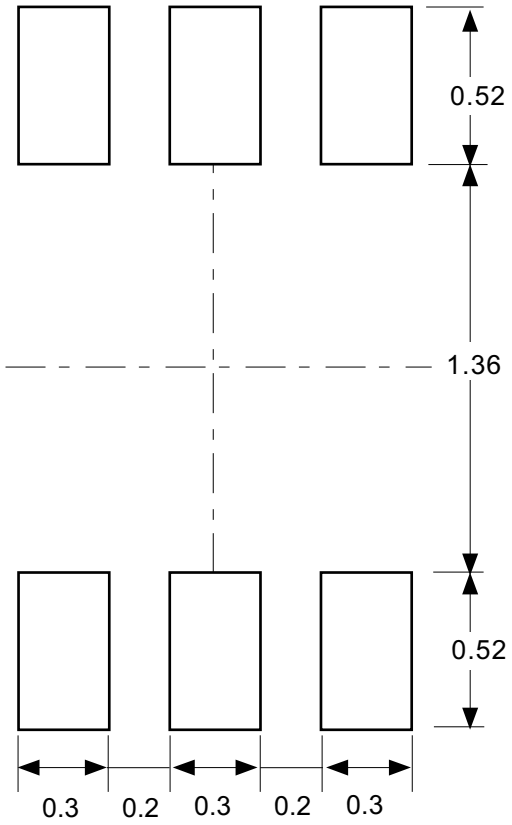



Enlarged drawing in the central part




No. PG006-A-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | SNT-6A-A-Reel | | |
| No. | PG006-A-R-SD-1.0 | | |
| SCALE | | QTY. | 5,000 |
| UNIT | mm | | |
| | | | |
| Seiko Instruments Inc. | | | |




Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がることがありますのでご配慮ください。

No. PG006-A-L-SD-3.0

| | |
|---|---|
| TITLE | SNT-6A-A-Land Recommendation |
| No. | PG006-A-L-SD-3.0 |
| SCALE | |
| UNIT | mm |
| | |
| Seiko Instruments Inc. | |

SII

Seiko Instruments Inc.
www.sii-ic.com

- The information described herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or diagrams described herein whose related industrial properties, patents, or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee the success of any specific mass-production design.
- When the products described herein are regulated products subject to the Wassenaar Arrangement or other agreements, they may not be exported without authorization from the appropriate governmental authority.
- Use of the information described herein for other purposes and/or reproduction or copying without the express permission of Seiko Instruments Inc. is strictly prohibited.
- The products described herein cannot be used as part of any device or equipment affecting the human body, such as exercise equipment, medical equipment, security systems, gas equipment, or any apparatus installed in airplanes and other vehicles, without prior written permission of Seiko Instruments Inc.
- Although Seiko Instruments Inc. exerts the greatest possible effort to ensure high quality and reliability, the failure or malfunction of semiconductor products may occur. The user of these products should therefore give thorough consideration to safety design, including redundancy, fire-prevention measures, and malfunction prevention, to prevent any accidents, fires, or community damage that may ensue.