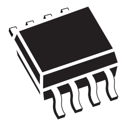
M95M02-DR

2 Mbit serial SPI bus EEPROM

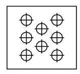
Preliminary data

Features

- Compatible with the Serial Peripheral Interface (SPI) bus
- Memory array
  - 2 Mb (256 Kbytes) of EEPROM
  - Page size: 256 bytes
- Additional Write lockable Page (Identification page)
- Write
  - Byte Write within 10 ms
  - Page Write within 10 ms
- Write Protect: quarter, half or whole memory array
- Clock frequency: 5 MHz
- Single supply voltage: 1.8 V to 5.5 V
- More than 1 million Write cycles
- More than 40-year data retention
- Enhanced ESD Protection
- Packages
  - ECOPACK2® (RoHS compliant and Halogen-free)



SO8N (MN)
150 mils width



WLCSP (CS)

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Contents

List of tables

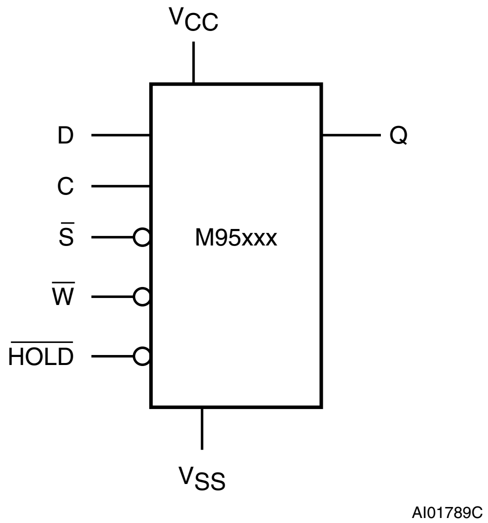
List of figures

1 Description

The M95M02-DR devices are electrically erasable programmable memory (EEPROM) devices. They are accessed by an SPI-compatible bus. Their memory array is organized as 262 144 × 8 bits. It can also be seen as 1024 pages of 256 bytes each.

The M95M02-DR devices also offer an additional page, named the Identification Page (256 bytes) which can be written and (later) permanently locked in Read-only mode. This Identification Page offers flexibility in the application board production line, as the Identification Page can be used to store unique identification parameters and/or parameters specific to the production line.

Figure 1. Logic diagram



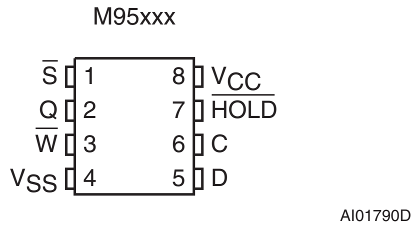
The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in *Table 1* and *Figure 1*.

The device is selected when Chip Select ($\overline{S}$) is taken low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

Table 1. Signal names

Signal name	Function	Direction
C	Serial Clock	Input
D	Serial Data Input	Input
Q	Serial Data Output	Output
S	Chip Select	Input
$\overline{W}$	Write Protect	Input
$\overline{HOLD}$	Hold	Input
V_{CC}	Supply voltage	
V_{SS}	Ground	

Figure 2. SO8N connections



1. See *Section 11: Package mechanical data* for package dimensions, and how to identify pin-1.

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 11*). These signals are described next.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data Output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

2.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all write instructions.

2.7 V_{CC} supply voltage

V_{CC} is the supply voltage.

2.8 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

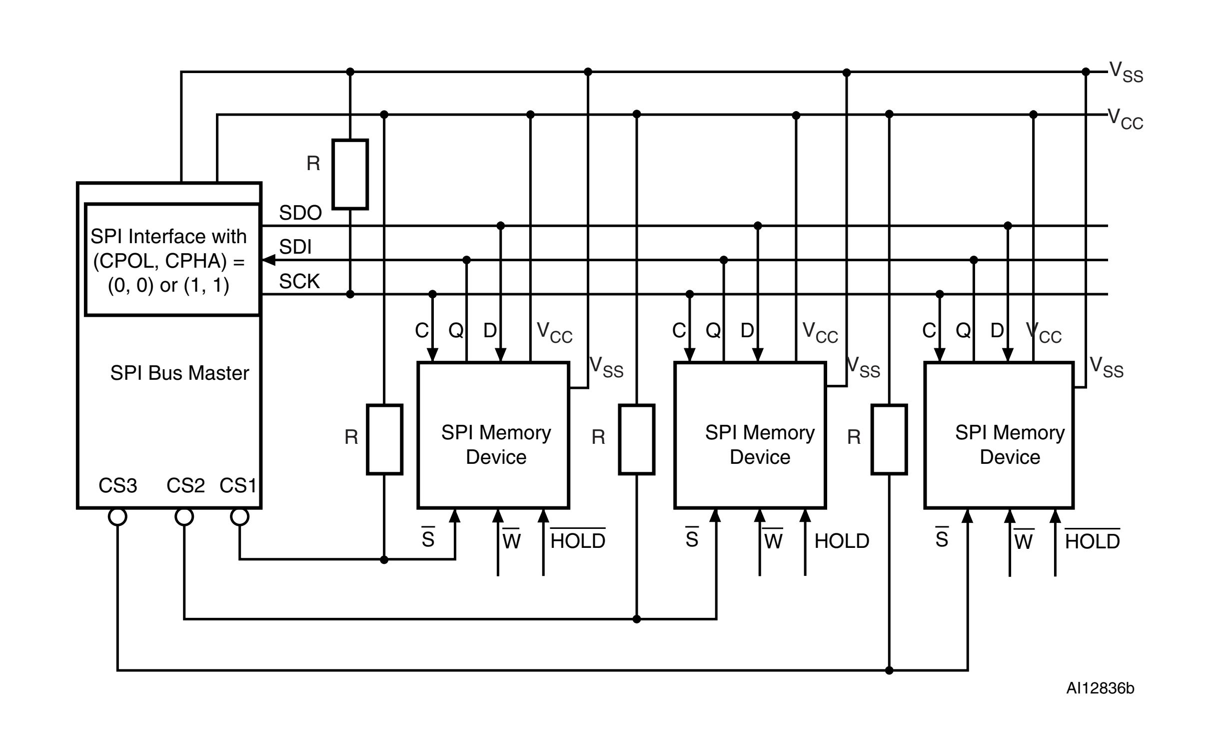
3 Connecting to the SPI bus

These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data Input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data Output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven high or low as appropriate.

Figure 3 shows an example of three memory devices connected to an MCU, on an SPI bus. Only one device is selected at a time, so only one device drives the Serial Data Output (Q) line at a time, the other devices are high impedance.

A pull-up resistor connected on each $\overline{S}$ input (represented in *Figure 3*) ensures that each device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

In applications where the bus master might enter a state where the whole input/output SPI bus is high-impedance at a given time (for example, if the bus master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high). This ensures that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met.

3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

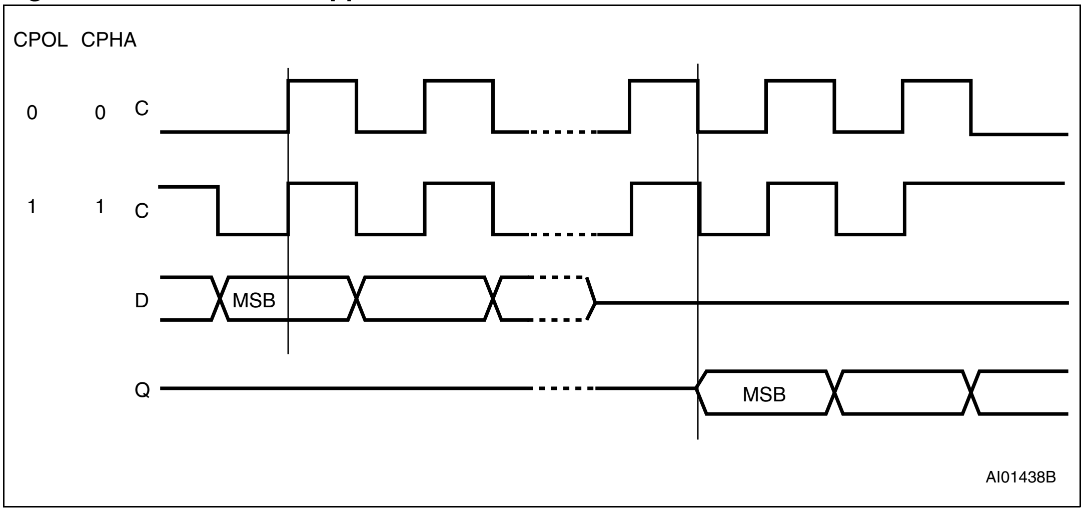
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Standby mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. SPI modes supported



4 Operating features

4.1 Supply voltage (V_{CC})

4.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8*.). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

4.1.2 Device reset

In order to prevent inadvertent write operations during power-up, a power on reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 8*.

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in Standby Power mode
- deselected (note that, to be executed, an instruction must be preceded by a falling edge on Chip Select ($\overline{S}$))
- Status Register value:
  – the Write Enable Latch (WEL) is reset to 0
  – Write In Progress (WIP) is reset to 0
  – The SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits)

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. The device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 8*.

4.1.3 Power-up conditions

When the power supply is turned on, V_{CC} rises continuously from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage, it is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 3*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 8* and the rise time must not vary faster than 1 V/µs.

4.1.4 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 8*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- in Standby Power mode (there should not be any internal write cycle in progress).

4.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}, as specified in *Table 11*.

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to I_{CC1}.

4.3 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data Output (Q) is high impedance, and Serial Data Input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

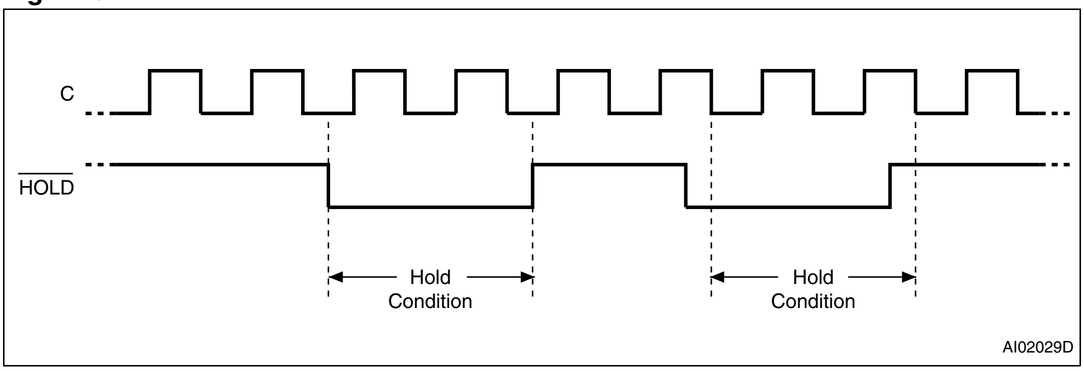
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven low at the same time as Serial Clock (C) already being low (as shown in *Figure 5*).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven high at the same time as Serial Clock (C) already being low.

Figure 5 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

Figure 5. Hold condition activation



4.4 Status Register

Figure 6 shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits

4.5 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{W}$) signal allows the Block Protect (BP1, BP0) bits of the Status Register to be protected.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points need to be noted in the previous sentence:

- The ‘last bit of the instruction’ can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The ‘next rising edge of Serial Clock (C)’ might (or might not) be the next bus transaction for some other device on the SPI bus.

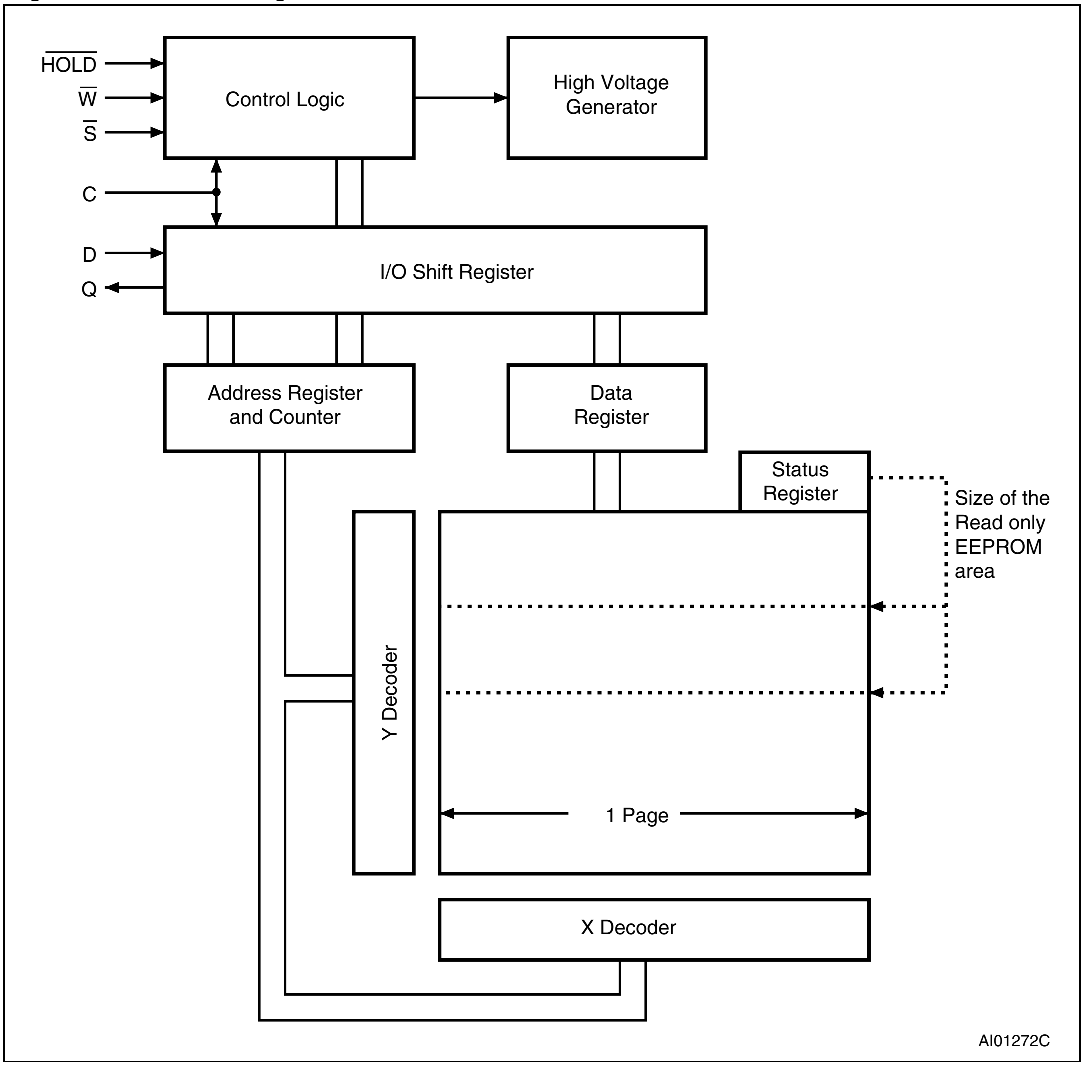
Table 2. Write-protected block size

Status Register bits		Protected block	Array addresses protected
BP1	BP0		
0	0	none	none
0	1	Upper quarter	3 0000h - 3 FFFFh
1	0	Upper half	2 0000h - 3 FFFFh
1	1	Whole memory	0 0000h - 3 FFFFh

5 Memory organization

The memory is organized as shown in *Figure 6*.

Figure 6. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in *Table 3*), the device automatically deselects itself.

Table 3. Instruction set

Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010
Read Identification Page	Reads the page dedicated to identification	1000 0011(1)
Write Identification Page	Writes the page dedicated to identification	1000 0010(1)
Read Lock Status	Reads the lock status of the Identification Page	1000 0011(2)
Lock ID	Locks the Identification page in read-only mode	1000 0010(2)

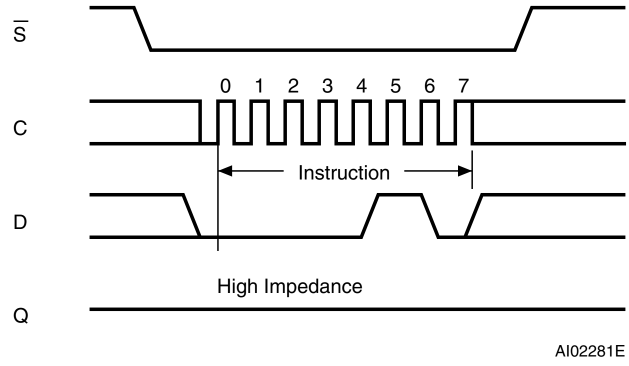
1. Address bit A10 must be 0, all other address bits are Don't Care.
2. Address bit A10 must be 1, all other address bits are Don't Care.

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 7. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

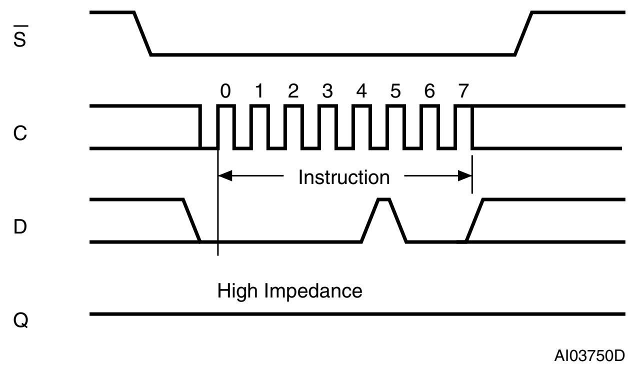
As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 9*.

The status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 4*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 4. Status Register format

b7							b0
SRWD	0	0	0	BP1	BP0	WEL	WIP

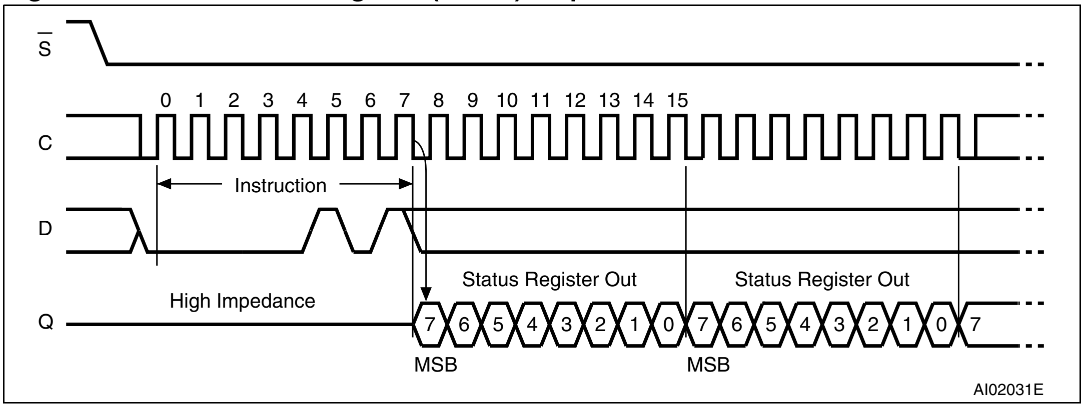
SRWD: Status Register Write Protect

BP1, BP0: Block Protect Bits

WEL: Write Enable Latch Bit

WIP: Write In Progress Bit

Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed. After the Write Enable (WREN) instruction has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, followed by the instruction code and the data byte on Serial Data Input (D).

The instruction sequence is shown in *Figure 10*.

The Write Status Register (WRSR) instruction has no effect on b6, b5, b4, b1 and b0 of the Status Register. b6, b5 and b4 are always read as 0.

Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not properly executed. As soon as Chip Select ($\overline{S}$) is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

Figure 10. Write Status Register (WRSR) sequence

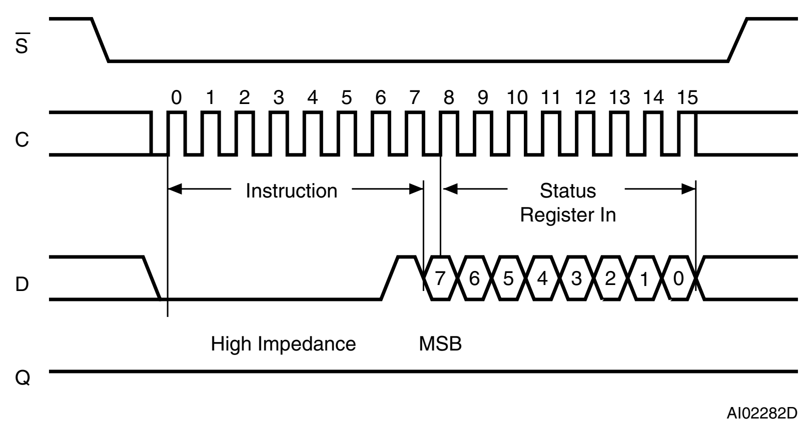


Table 5. Protection modes

W̄ Signal	SRWD Bit	Mode	Write Protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software Protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write Protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware Protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Write Protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *Table 5*.

The Write Status Register (WRSR) instruction allows the user to change the values of the Block Protect (BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in *Table 4*.

The Write Status Register (WRSR) instruction also allows the user to set or reset the Status Register Write Disable (SRWD) bit in accordance with the Write Protect (W̄) signal. The Status Register Write Disable (SRWD) bit and Write Protect (W̄) signal allow the device to be put in the Hardware Protected Mode (HPM). The Write Status Register (WRSR) instruction is not executed once the Hardware Protected Mode (HPM) is entered.

The contents of the Status Register Write Disable (SRWD) and Block Protect (BP1, BP0) bits are frozen at their current values from just before the start of the execution of Write Status Register (WRSR) instruction. The new, updated, values take effect at the moment of completion of the execution of Write Status Register (WRSR) instruction.

The protection features of the device are summarized in *Table 2*.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of the whether Write Protect ($\overline{W}$) is driven high or low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect ($\overline{W}$) is driven low, it is *not* possible to write to the Status Register *even* if the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software protected (SPM) by the Block Protect (BP1, BP0) bits of the Status Register, are also hardware protected against data modification.

Regardless of the order of the two events, the Hardware Protected Mode (HPM) can be entered:

- by setting the Status Register Write Disable (SRWD) bit after driving Write Protect ($\overline{W}$) low
- or by driving Write Protect ($\overline{W}$) low after setting the Status Register Write Disable (SRWD) bit.

The only way to exit the Hardware Protected Mode (HPM) once entered is to pull Write Protect ($\overline{W}$) high.

If Write Protect ($\overline{W}$) is permanently tied high, the Hardware Protected Mode (HPM) can never be activated, and only the Software Protected Mode (SPM), using the Block Protect (BP1, BP0) bits of the Status Register, can be used.

6.5 Read from Memory Array (READ)

As shown in *Figure 11*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

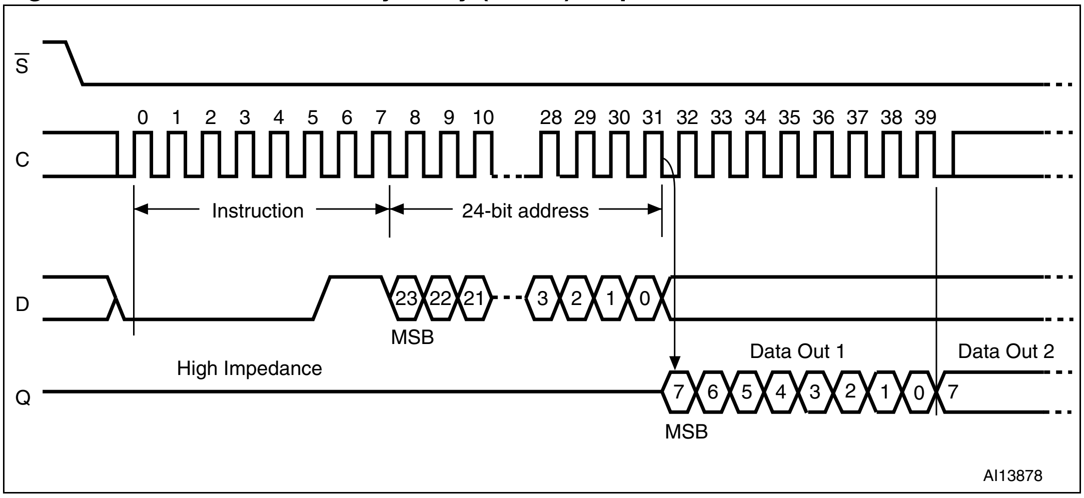
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 11. Read from Memory Array (READ) sequence



1. As shown in *Table 6*, the most significant address bits are Don't Care.

Table 6. Address range bits(1)

M95M02-DR	
Address bits	A17-A0

1. Bits A23 to A18 are Don't Care.

6.6 Read Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode.

Reading this page is achieved with the Read Identification Page instruction (see *Table 3*). The Chip Select signal (S) is first driven low, the bits of the instruction byte and address bytes are then shifted in, on Serial Data input (D). Address bit A10 must be 0, address bits [A17:A11] and [A9:A8] are Don't Care, and the data byte pointed to by [A7:A0] is shifted out on Serial Data output (Q).

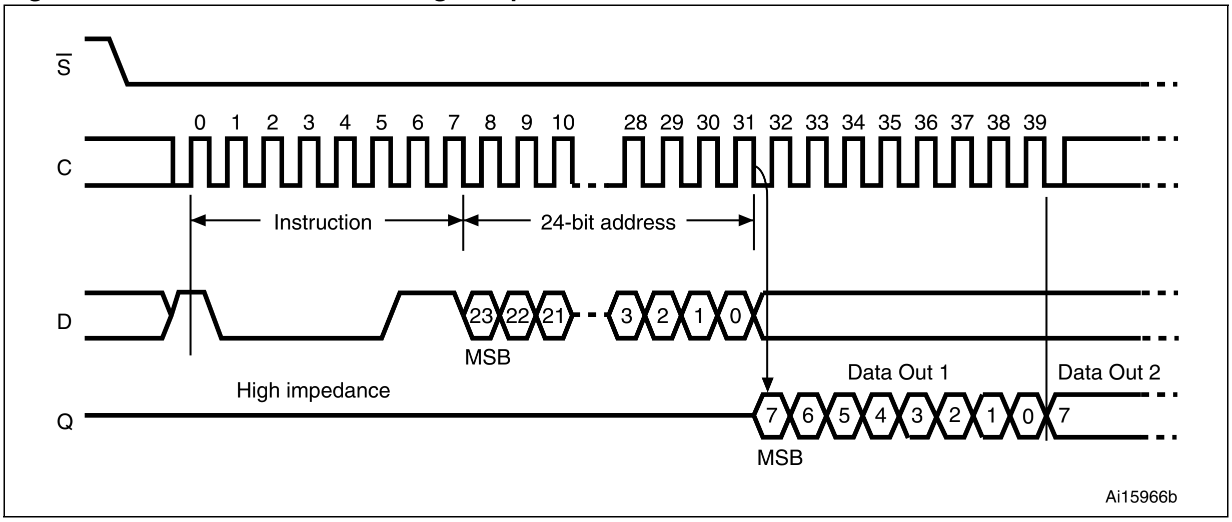
If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

Note: The number of bytes to read from the ID page must not exceed the page boundary (e.g.: when reading the ID page from location 100d, the number of bytes should be less than or equal to 156d, as the ID page is 256 bytes wide).

The read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle. The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a write cycle is currently in progress.

Figure 12. Read Identification Page sequence



6.7 Write to Memory Array (WRITE)

As shown in *Figure 13*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. In the case of *Figure 13*, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts, and continues for a period t_{WC} (as specified in *Table 12*), at the end of which the Write in Progress (WIP) bit is reset to 0.

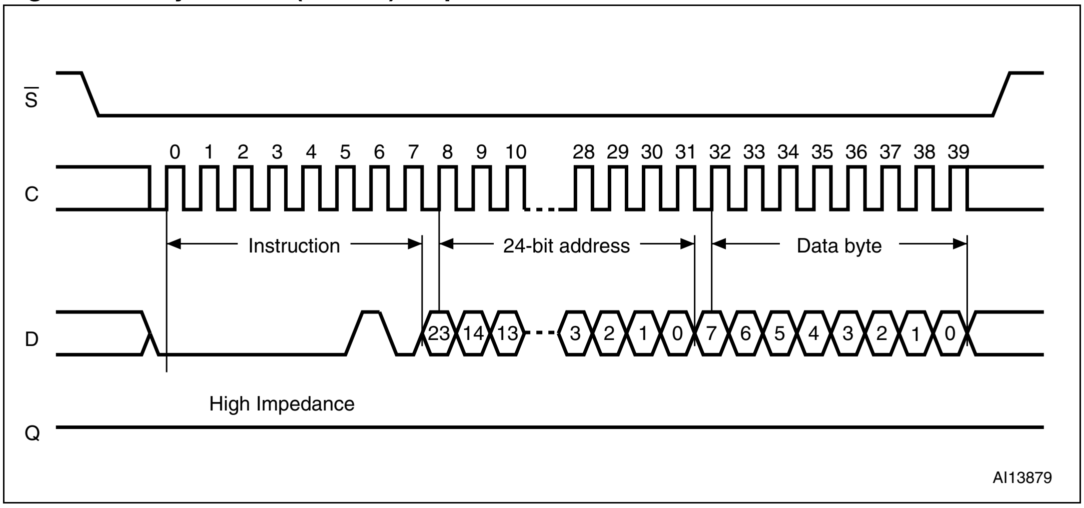
If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 14*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle. The self-timed Write cycle starts, and continues, for a period t_{WC} (as specified in *Table 12*), at the end of which the Write in Progress (WIP) bit is reset to 0.

Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size is 256 bytes).

The instruction is not accepted, and is not executed, under the following conditions:
- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a Write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

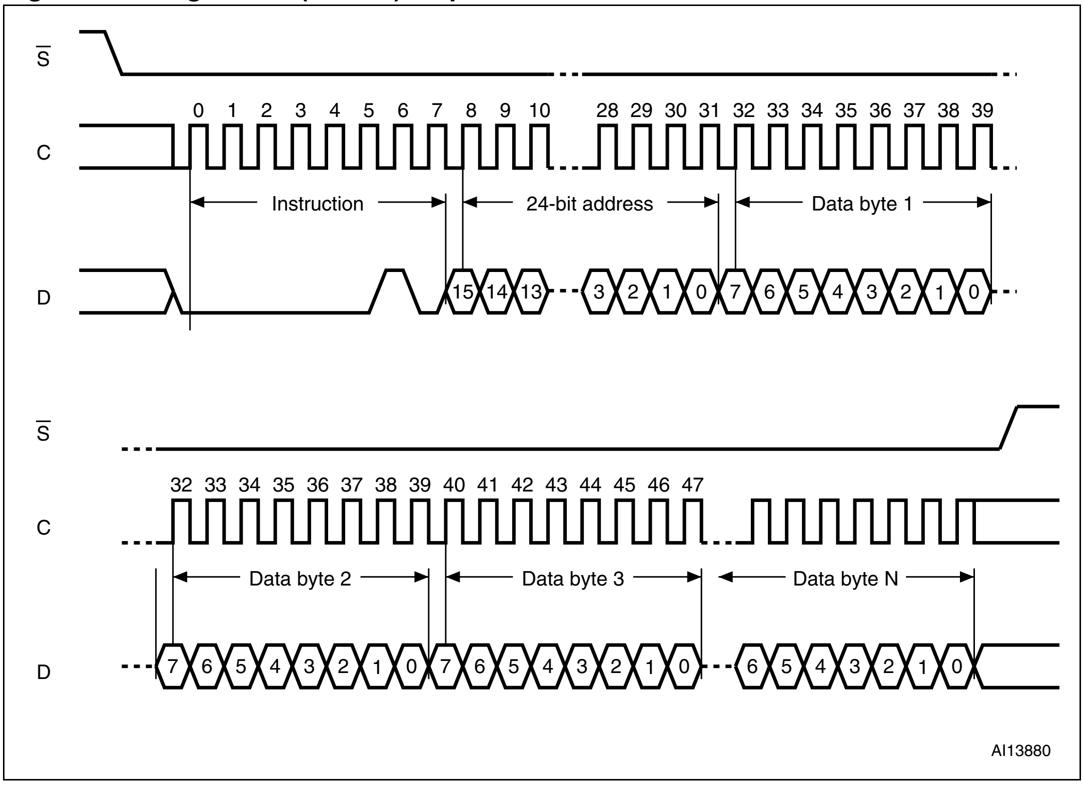
Note: The self-timed write cycle, t_W, is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as “0” and a programmed bit is read as “1”.

Figure 13. Byte Write (WRITE) sequence



1. As shown in *Table 6*, the most significant address bits are Don’t Care.

Figure 14. Page Write (WRITE) sequence



1. As shown in *Table 6*, the most significant address bits are Don't Care.

6.8 Write Identification Page

The Identification Page (256 bytes) is an additional page which can be written and (later) permanently locked in Read-only mode. Writing this page is achieved with the Write Identification Page instruction (see *Table 3*), the Chip Select signal (S) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in on Serial Data input (D). Address bit A10 must be 0, address bits [A23:A11] and [A9:A8] are Don't Care, the [A7:A0] address bits define the byte address inside the identification page.

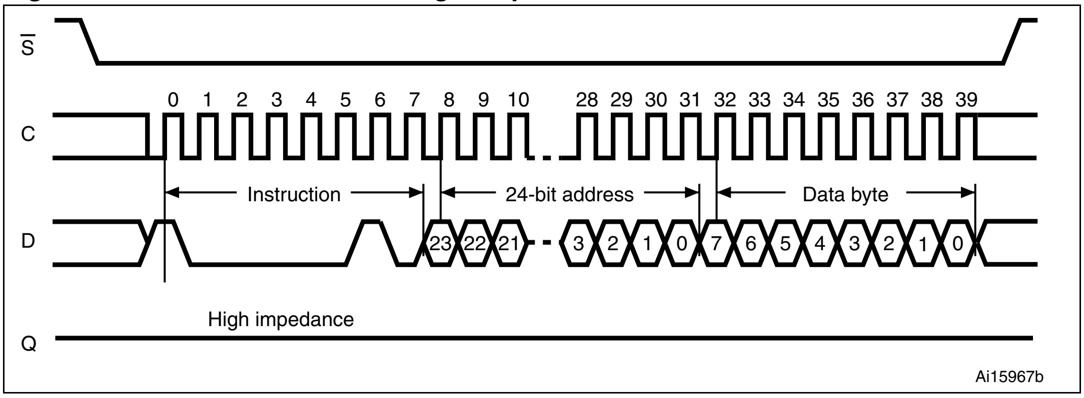
The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. The self-timed write cycle triggered by the rising edge of Chip Select ($\overline{S}$) continues for a period t_W (as specified in *Table 12*), at the end of which the Write in Progress (WIP) bit is reset to 0.

In the case of *Figure 15*, Chip Select ($\overline{S}$) is driven high after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. However, if Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 15*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal write cycle. Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented.

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by previously executing a Write Enable instruction)
- if Status register bits (BP1, BP0) = (1, 1)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that was latched in)
- if the Identification page is locked by the Lock Status bit

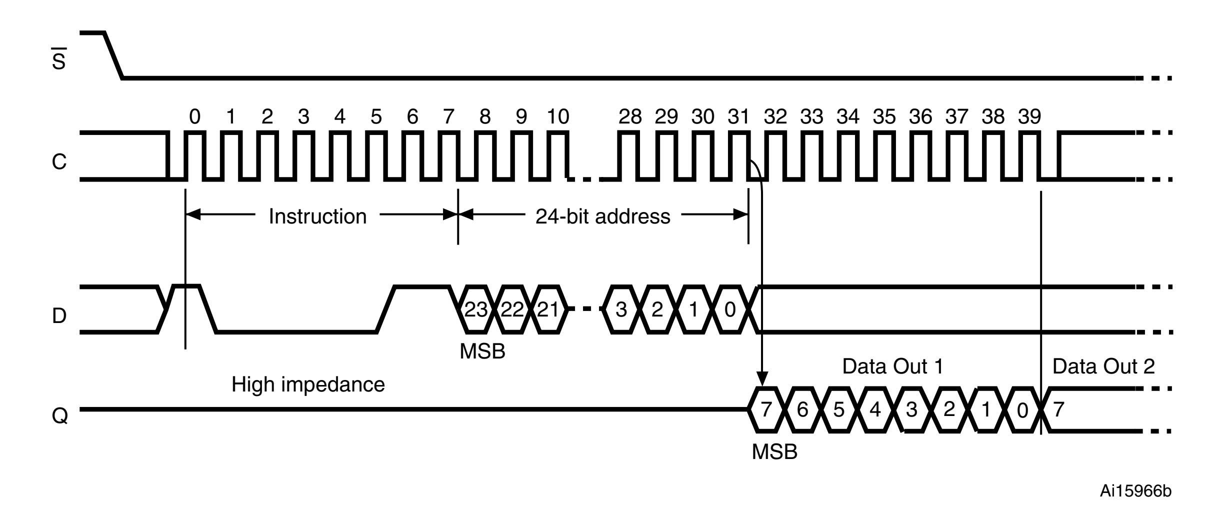
Figure 15. Write Identification Page sequence



6.9 Read Lock Status

The Read Lock Status instruction (see *Table 3*) is used to check if the Identification Page is locked (or not) in read-only mode. The Read Lock Status sequence is defined with the Chip Select (S) first driven low. The bits of the instruction byte and address bytes are then shifted in on Serial Data input (D). Address bit A10 must be 1, all other address bits are Don't Care. The Lock bit is the LSB (least significant bit) of the byte read on Serial Data output (Q). It is at '1' when the lock is active and at '0' when the lock is not active. If Chip Select ($\overline{S}$) continues to be driven low, the same data byte is shifted out. The read cycle is terminated by driving Chip Select ($\overline{S}$) high.

Figure 16. Read Lock Status sequence



6.10 Lock ID

The Lock ID instruction permanently locks the Identification Page in read-only mode. Before this instruction can be accepted, a Write Enable (WREN) instruction must have been executed. The Lock ID instruction (see *Table 3*) is issued by driving Chip Select ($\overline{S}$) low, sending the instruction code, the address and a data byte on Serial Data input (D), and driving Chip Select ($\overline{S}$) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care.

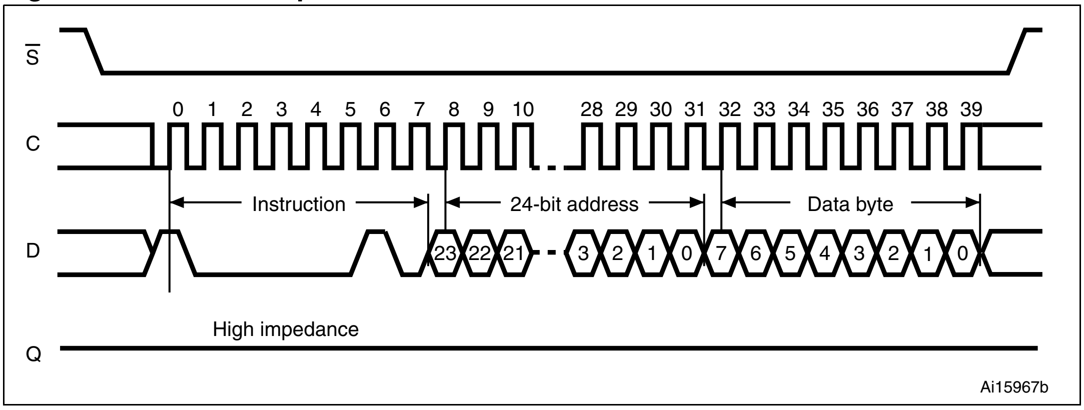
Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Lock ID instruction is not executed.

Driving Chip Select ($\overline{S}$) high at a byte boundary of the input data triggers the self-timed write cycle whose duration is t_W (specified in *Table 12*).

The instruction is not accepted, and so not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by previously executing a Write Enable instruction)
- if Status register bits (BP1,BP0) = (1,1)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that was latched in)
- if the Identification page is locked by the Lock Status bit

Figure 17. Lock ID sequence



7 ECC (error correction code) and write cycling

The M95M02-DR devices offer an ECC (error correction code) logic which compares each 4-byte word with its associated 6 EEPROM bits of ECC. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note, however, that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC bits), that is, the addressed byte is cycled together with the other three bytes making up the word. It is therefore recommended to write data by word (4 bytes) at address 4*N (where N is an integer) in order to benefit from the larger amount of Write cycles.

Those devices are qualified at 1 million (1 000 000) write cycles, using a cycling routine that writes to the device by multiples of 4-byte packets.

8 Power-up and delivery state

8.1 Power-up state

After power-up, the device is in the following state:

- Standby Power mode
- Deselected (after power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).
- Not in the Hold condition
- Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

8.2 Initial delivery state

The device is delivered with the memory array set at all 1s (FFh). The Status Register Write Disable (SRWD) and Block Protect (BP1 and BP0) bits are initialized to 0.

9 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
	Ambient temperature with power applied	–40	130	°C
T_{STG}	Storage temperature	–65	150	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
V_{CC}	Supply voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)		5	mA
I_{OH}	DC output current (Q = 1)		–5	mA
V_{ESD}	Electrostatic discharge voltage (human body model)(2)		3000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU

2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500Ω, R2=500Ω)

10 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 9. AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF
	Input rise and fall times		25	ns
	Input pulse voltages	$0.2 V_{CC}$ to $0.8 V_{CC}$		V
	Input and output timing reference voltages	$0.3 V_{CC}$ to $0.7 V_{CC}$		V

Figure 18. AC measurement I/O waveform

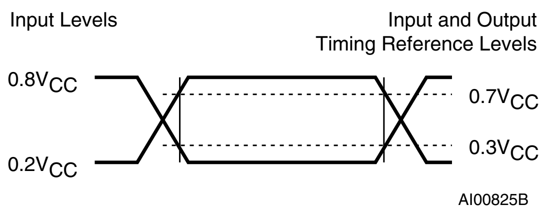


Table 10. Capacitance(1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	$V_{OUT} = 0$ V		8	pF
C_{IN}	Input capacitance (D)	$V_{IN} = 0$ V		8	pF
	Input capacitance (other pins)	$V_{IN} = 0$ V		6	pF

1. Not 100% tested.

Table 11. DC characteristics

Symbol	Parameter	Test condition (in addition to the conditions defined in *Table 8*)	Min	Max	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current (Read)	C = 0.1 V_{CC}/0.9 V_{CC} at 5 MHz, 1.8 V ≤ V_{CC} ≤ 5.5 V, Q = open		3	mA
I_{CC0}(1)	Supply current (Write)	During t_W, $\overline{S} = V_{CC}$,		3	mA
I_{CC1}	Supply current (Standby Power mode)	$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		3	µA
		$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, 1.8 V ≤ V_{CC} < 2.5 V		5	µA
		$\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}, 2.5 V ≤ V_{CC} ≤ 5.5 V		5	µA
V_{IL}	Input low voltage	1.8 V ≤ V_{CC} < 2.5 V	–0.45	0.25 V_{CC}	V
		2.5 V ≤ V_{CC} ≤ 5.5 V	–0.45	0.3 V_{CC}	
V_{IH}	Input high voltage	1.8 V ≤ V_{CC} < 2.5 V	0.75 V_{CC}	V_{CC}+1	V
		2.5 V ≤ V_{CC} ≤ 5.5 V	0.7 V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	I_{OL} = 0.15 mA, V_{CC} = 1.8 V		0.3	V
		V_{CC} = 2.5 V, I_{OL} = 1.5 mA or V_{CC} = 5 V, I_{OL} = 2 mA		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.1 mA, V_{CC} = 1.8 V	0.8 V_{CC}		V
		V_{CC} = 2.5 V, I_{OH} = –0.4 mA or V_{CC} = 5 V, I_{OH} = –2 mA			

1. Characterized value, not tested in production.

Table 12. AC characteristics

Test conditions specified in *Table 8* and *Table 9*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	60		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	60		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	90		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	60		ns
t_{CHSL}		$\overline{S}$ not active hold time	60		ns
t_{CH} (1)	t_{CLH}	Clock high time	90		ns
t_{CL} (1)	t_{CLL}	Clock low time	90		ns
t_{CLCH} (2)	t_{RC}	Clock rise time		2	µs
t_{CHCL} (2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		ns
t_{CHDX}	t_{DH}	Data in hold time	20		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	60		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	60		ns
t_{CLHL}		Clock low setup time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low setup time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ} (2)	t_{DIS}	Output Disable time		80	ns
t_{CLQV} (3)	t_V	Clock low to output valid		80	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH} (2)	t_{RO}	Output rise time		80	ns
t_{QHQL} (2)	t_{FO}	Output fall time		80	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		80	ns
t_{HLQZ} (2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		80	ns
t_W	t_{WC}	Write time		10	ms

1. $t_{CH} + t_{CL}$ must never be less than the shortest possible clock period, $1 / f_C(max)$
2. Value guaranteed by characterization, not 100% tested in production.
3. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a read setup time t_{SU} = 0 ns, t_{CL} can be equal to (or greater than) t_{CLQV}; in all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV} + t_{SU}$.

Figure 19. Serial input timing

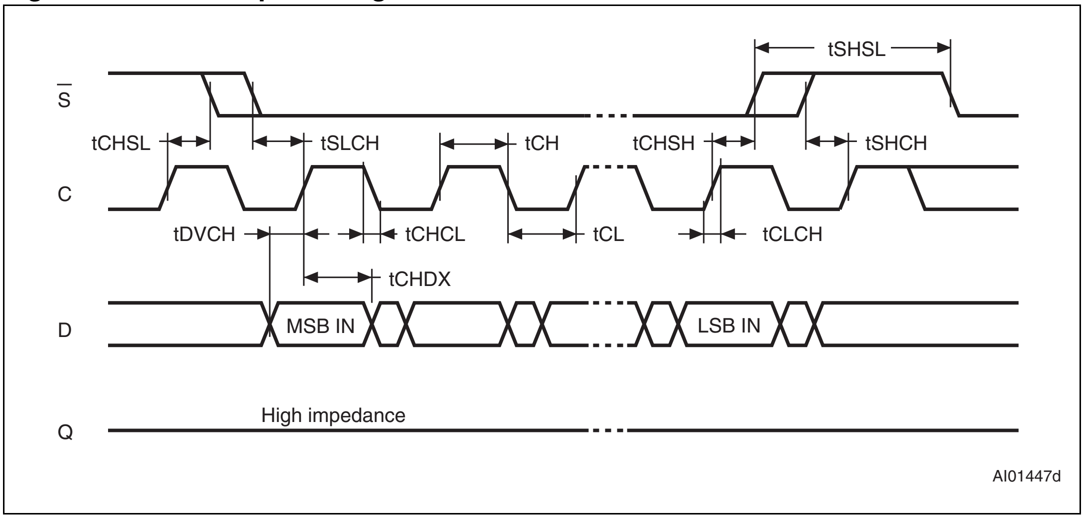


Figure 20. Hold timing

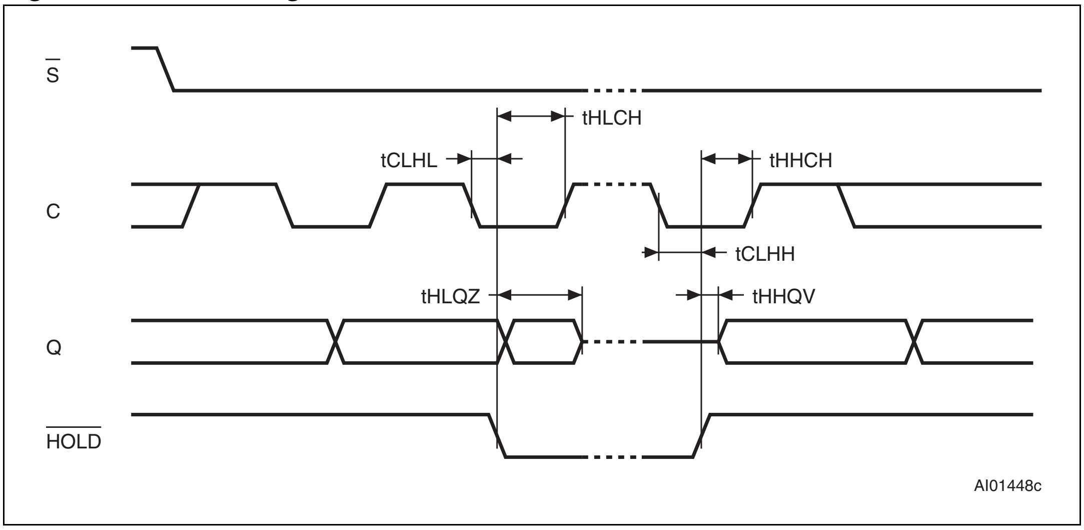
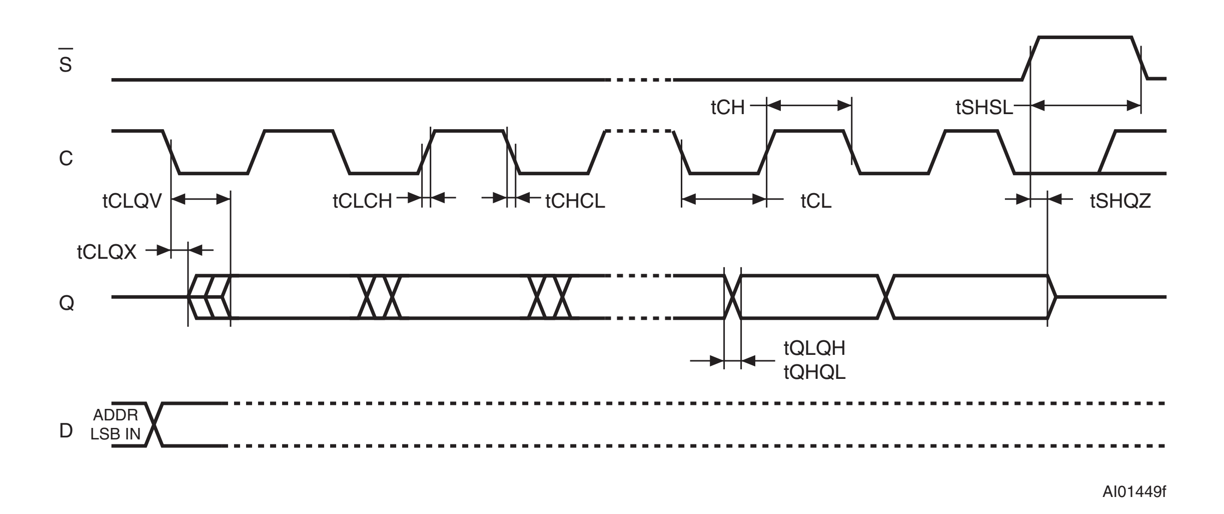


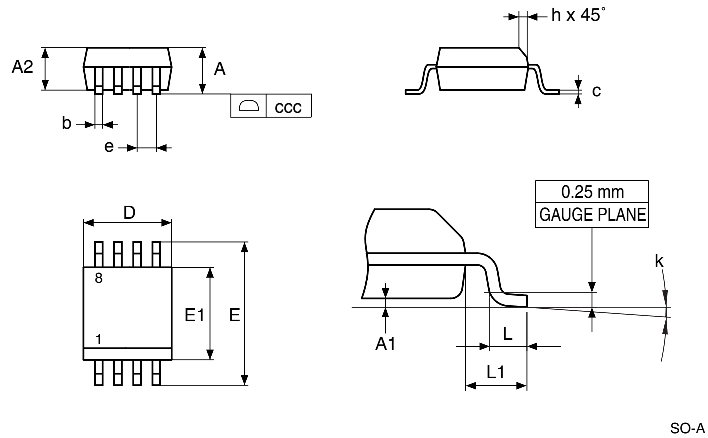
Figure 21. Serial output timing



11 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 22. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline



1. Drawing is not to scale.

Table 13. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches(1)		
	Typ	Min	Max	Typ	Min	Max
A			1.750			0.0689
A1		0.100	0.250		0.0039	0.0098
A2		1.250			0.0492	
b		0.280	0.480		0.0110	0.0189
c		0.170	0.230		0.0067	0.0091
ccc			0.100			0.0039
D	4.900	4.800	5.000	0.1929	0.1890	0.1969
E	6.000	5.800	6.200	0.2362	0.2283	0.2441
E1	3.900	3.800	4.000	0.1535	0.1496	0.1575
e	1.270	–	–	0.0500	-	-
h		0.250	0.500		0.0098	0.0197
k		0°	8°		0°	8°
L		0.400	1.270		0.0157	0.0500
L1	1.040			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 23. M95M02-D WLCSP package outline

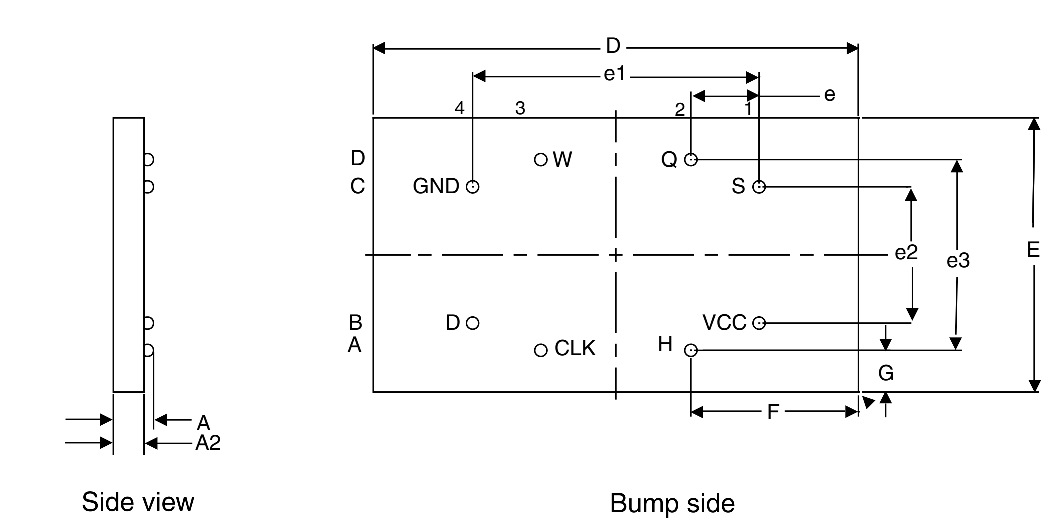


Table 14. M95M02-D WLCSP package mechanical data

Symbol	millimeters			inches[(1)]		
	Typ	Min	Max	Typ	Min	Max
A	0.295	0.265	0.325	0.0116	0.0104	0.0128
A2	0.225	0.210	0.240	0.0089	0.0083	0.0094
B (ball diam)	0.090	0.065	0.115	0.0035	0.0026	0.0045
D	3.556	3.536	3.576	0.1400	0.1392	0.1408
E	2.011	1.991	2.031	0.0792	0.0784	0.0800
e	0.500			0.0197		
e1	2.100			0.0827		
e2	1.000			0.0394		
e3	1.400			0.0551		
F	1.228			0.0483		
G	0.306			0.0120		
N	8					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

12 Part numbering

Table 15. Ordering information scheme

Example:	M95M02-D	R	MN	6	T	P

Device type

M95 = SPI serial access EEPROM

Device function

M02-D = 2048 Kbits (262 144 × 8) EEPROM with additional identification page

Operating voltage

R = V_{CC} = 1.8 V to 5.5 V

Package

MN = SO8N (150 mils width)

CS = WLCSP

Device grade

6 = Industrial temperature range, –40 to 85 °C.
Device tested with standard test flow

Option

blank = standard packing

T = tape and reel packing

Plating technology

P or G = ECOPACK2® (RoHS compliant and Halogen-free)

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

13 Revision history

Table 16. Document revision history

Date	Revision	Changes
15-Nov-2010	1	Initial release.
10-Dec-2010	2	Updated DC and AC characteristics according to characterization test results.
10-Jan-2011	3	Updated ordering information.
10-May-2011	4	Updated *Table 12: AC characteristics* and related text, and *Table 11: DC characteristics*.

Please Read Carefully:

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com