M95640
M95640-W M95640-R

64 Kbit serial SPI bus EEPROMs with high-speed clock

Features

- Compatible with SPI bus serial interface (positive clock SPI modes)
- Single supply voltage:
  - 4.5 to 5.5 V for M95640
  - 2.5 to 5.5 V for M95640-W
  - 1.8 to 5.5 V for M95640-R
- 10 MHz, 5 MHz or 2 MHz clock rates
- 5 ms write time
- Status Register
- Hardware protection of the Status Register
- Byte and Page Write (up to 32 bytes)
- Self-timed programming cycle
- Adjustable size read-only EEPROM area
- Enhanced ESD protection
- More than 1 million Write cycles
- More than 40-year data retention
- Packages
  - ECOPACK2® (RoHS-compliant and Halogen-free)

SO8 (MN)
150 mil width

TSSOP8 (DW)
169 mil width

UFDFPN8 (MB)
2 x 3 mm

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1 Description

The M95640, M95640-W and M95640-R are electrically erasable programmable memory (EEPROM) devices. They are accessed by a high-speed SPI-compatible bus. The devices are 64 Kbit devices organized as 8192 × 8 bits.

The device is accessed by a simple serial interface that is SPI-compatible. The bus signals are C, D and Q, as shown in *Table 1* and *Figure 1*.

The device is selected when Chip Select ($\overline{S}$) is taken low. Communications with the device can be interrupted using Hold ($\overline{HOLD}$).

Figure 1. Logic diagram

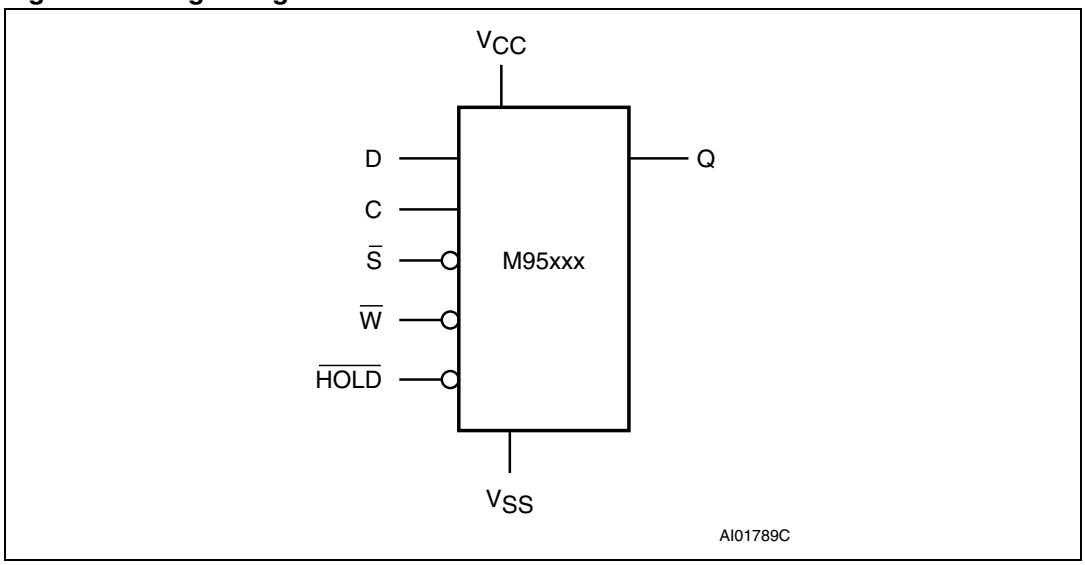
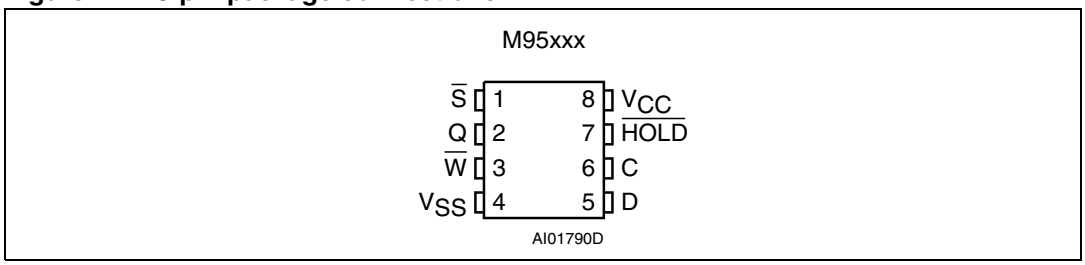


Figure 2. 8-pin package connections



1. See *Package mechanical data* section for package dimensions and how to identify pin-1.

Table 1. Signal names

Signal name	Description
C	Serial Clock
D	Serial data input
Q	Serial data output
$\overline{S}$	Chip Select
$\overline{W}$	Write Protect
$\overline{HOLD}$	Hold
V_{CC}	Supply voltage
V_{SS}	Ground

2 Signal description

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC}(min) to V_{CC}(max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}, as specified in *Table 13* to *Table 16*). These signals are described next.

2.1 Serial Data output (Q)

This output signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (C).

2.2 Serial Data input (D)

This input signal is used to transfer data serially into the device. It receives instructions, addresses, and the data to be written. Values are latched on the rising edge of Serial Clock (C).

2.3 Serial Clock (C)

This input signal provides the timing of the serial interface. Instructions, addresses, or data present at Serial Data Input (D) are latched on the rising edge of Serial Clock (C). Data on Serial Data Output (Q) changes after the falling edge of Serial Clock (C).

2.4 Chip Select ($\overline{S}$)

When this input signal is high, the device is deselected and Serial Data output (Q) is at high impedance. Unless an internal Write cycle is in progress, the device will be in the Standby Power mode. Driving Chip Select ($\overline{S}$) low selects the device, placing it in the Active Power mode.

After Power-up, a falling edge on Chip Select ($\overline{S}$) is required prior to the start of any instruction.

2.5 Hold ($\overline{HOLD}$)

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without deselecting the device.

During the Hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are Don't Care.

To start the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) driven low.

2.6 Write Protect ($\overline{W}$)

The main purpose of this input signal is to freeze the size of the area of memory that is protected against Write instructions (as specified by the values in the BP1 and BP0 bits of the Status Register).

This pin must be driven either high or low, and must be stable during all write operations.

2.7 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.8 V_{CC} supply voltage

Refer to *Section 4.1: Supply voltage (V_{CC}) on page 12*.

3 Connecting to the SPI bus

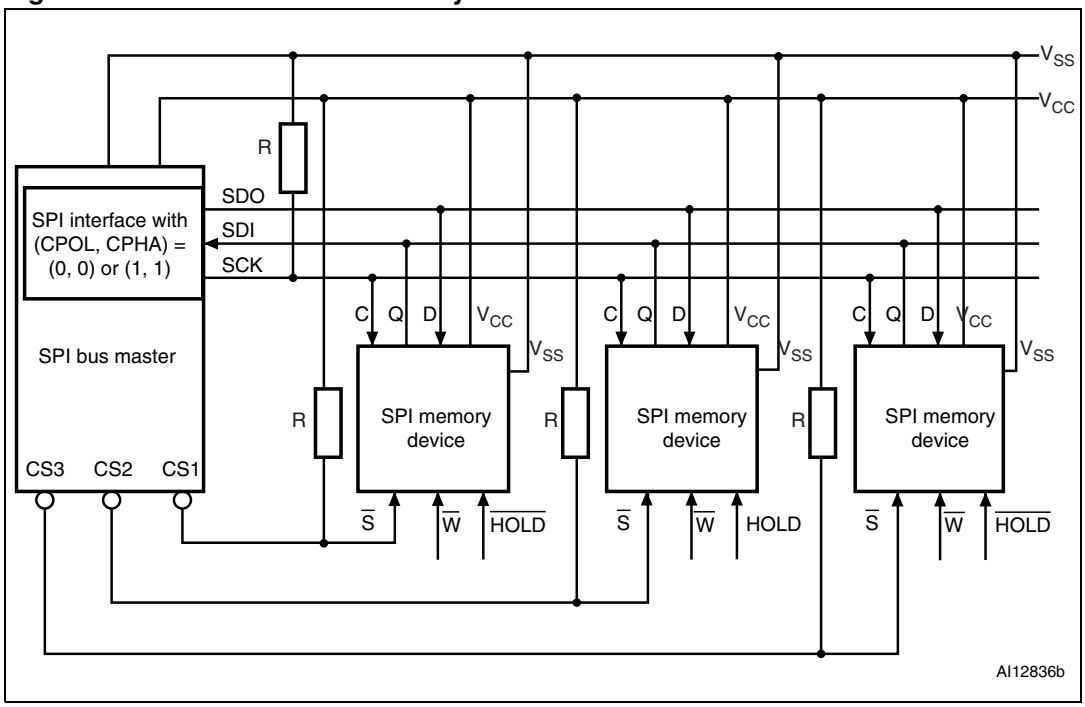
These devices are fully compatible with the SPI protocol.

All instructions, addresses and input data bytes are shifted in to the device, most significant bit first. The Serial Data input (D) is sampled on the first rising edge of the Serial Clock (C) after Chip Select ($\overline{S}$) goes low.

All output data bytes are shifted out of the device, most significant bit first. The Serial Data output (Q) is latched on the first falling edge of the Serial Clock (C) after the instruction (such as the Read from Memory Array and Read Status Register instructions) have been clocked into the device.

Figure 3 shows three devices, connected to an MCU, on a SPI bus. Only one device is selected at a time, so only one device drives the Serial Data output (Q) line at a time, all the others being high impedance.

Figure 3. Bus master and memory devices on the SPI bus



1. The Write Protect ($\overline{W}$) and Hold ($\overline{HOLD}$) signals should be driven, high or low as appropriate.

The pull-up resistor R (represented in *Figure 3*) ensures that a device is not selected if the bus master leaves the $\overline{S}$ line in the high impedance state.

In applications where the bus master might enter a state where all inputs/outputs SPI bus would be in high impedance at the same time (for example, if the bus master is reset during the transmission of an instruction), the clock line (C) must be connected to an external pull-down resistor so that, if all inputs/outputs become high impedance, the C line is pulled low (while the $\overline{S}$ line is pulled high): this will ensure that $\overline{S}$ and C do not become high at the same time, and so, that the t_{SHCH} requirement is met. The typical value of R is 100 kΩ.

3.1 SPI modes

These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

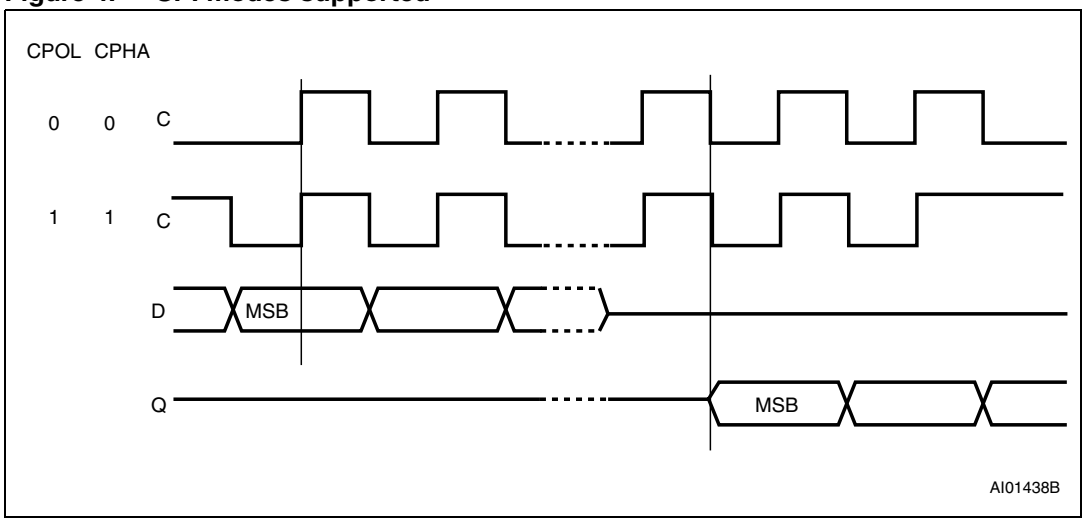
- CPOL=0, CPHA=0
- CPOL=1, CPHA=1

For these two modes, input data is latched in on the rising edge of Serial Clock (C), and output data is available from the falling edge of Serial Clock (C).

The difference between the two modes, as shown in *Figure 4*, is the clock polarity when the bus master is in Stand-by mode and not transferring data:

- C remains at 0 for (CPOL=0, CPHA=0)
- C remains at 1 for (CPOL=1, CPHA=1)

Figure 4. SPI modes supported



4 Operating features

4.1 Supply voltage (V_{CC})

4.1.1 Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 8*, *Table 9* and *Table 10*). This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

4.1.2 Device reset

In order to prevent inadvertent write operations during power-up, a power-on-reset (POR) circuit is included. At power-up, the device does not respond to any instruction until V_{CC} reaches the internal threshold voltage (this threshold is defined in DC characteristics tables *13*, *14*, *15* and *16* as V_{RES}).

When V_{CC} passes over the POR threshold, the device is reset and in the following state:

- in the Standby Power mode
- deselected (note that, to be executed, an instruction must be preceded by a falling edge on Chip Select ($\overline{S}$))
- Status register values:
  - the Write Enable Latch (WEL) bit is reset to 0
  - the Write In Progress (WIP) bit is reset to 0
  - the SRWD, BP1 and BP0 bits remain unchanged (non-volatile bits).

When V_{CC} passes over the POR threshold, the device is reset and enters the Standby Power mode. The device must not be accessed until V_{CC} reaches a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range defined in *Table 8*, *Table 9* and *Table 10*.

4.1.3 Power-up conditions

When the power supply is turned on, V_{CC} continuously rises from V_{SS} to V_{CC}. During this time, the Chip Select ($\overline{S}$) line is not allowed to float but should follow the V_{CC} voltage. It is therefore recommended to connect the $\overline{S}$ line to V_{CC} via a suitable pull-up resistor (see *Figure 3*).

In addition, the Chip Select ($\overline{S}$) input offers a built-in safety feature, as the $\overline{S}$ input is edge-sensitive as well as level-sensitive: after power-up, the device does not become selected until a falling edge has first been detected on Chip Select ($\overline{S}$). This ensures that Chip Select ($\overline{S}$) must have been high, prior to going low to start the first operation.

The V_{CC} voltage has to rise continuously from 0 V up to the minimum V_{CC} operating voltage defined in *Table 8*, *Table 9* and *Table 10* and the rise time must not vary faster than 1 V/µs.

4.1.4 Power-down

During power-down (continuous decrease in the V_{CC} supply voltage below the minimum V_{CC} operating voltage defined in *Table 8*, *Table 9* and *Table 10*), the device must be:

- deselected (Chip Select $\overline{S}$ should be allowed to follow the voltage applied on V_{CC})
- in Standby Power mode (there should not be any internal write cycle in progress).

4.2 Active Power and Standby Power modes

When Chip Select ($\overline{S}$) is low, the device is selected, and in the Active Power mode. The device consumes I_{CC}, as specified in *Table 13* to *Table 16*.

When Chip Select ($\overline{S}$) is high, the device is deselected. If a Write cycle is not currently in progress, the device then goes in to the Standby Power mode, and the device consumption drops to I_{CC1}.

4.2.1 Hold condition

The Hold ($\overline{HOLD}$) signal is used to pause any serial communications with the device without resetting the clocking sequence.

During the Hold condition, the Serial Data output (Q) is high impedance, and Serial Data input (D) and Serial Clock (C) are Don't Care.

To enter the Hold condition, the device must be selected, with Chip Select ($\overline{S}$) low.

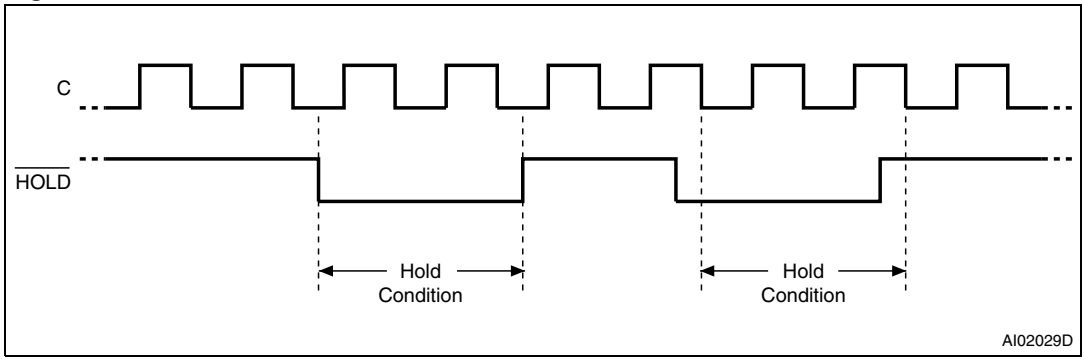
Normally, the device is kept selected, for the whole duration of the Hold condition. Deselecting the device while it is in the Hold condition, has the effect of resetting the state of the device, and this mechanism can be used if it is required to reset any processes that had been in progress.

The Hold condition starts when the Hold ($\overline{HOLD}$) signal is driven low at the same time as Serial Clock (C) already being low (as shown in *Figure 5*).

The Hold condition ends when the Hold ($\overline{HOLD}$) signal is driven high at the same time as Serial Clock (C) already being low.

Figure 5 also shows what happens if the rising and falling edges are not timed to coincide with Serial Clock (C) being low.

Figure 5. Hold condition activation



4.3 Status Register

Figure 6 shows the position of the Status Register in the control logic of the device. The Status Register contains a number of status and control bits that can be read or set (as appropriate) by specific instructions. See *Section 6.3: Read Status Register (RDSR)* for a detailed description of the Status Register bits.

4.4 Data protection and protocol control

Non-volatile memory devices can be used in environments that are particularly noisy, and within applications that could experience problems if memory bytes are corrupted. Consequently, the device features the following data protection mechanisms:

- Write and Write Status Register instructions are checked that they consist of a number of clock pulses that is a multiple of eight, before they are accepted for execution.
- All instructions that modify data must be preceded by a Write Enable (WREN) instruction to set the Write Enable Latch (WEL) bit. This bit is returned to its reset state by the following events:
  - Power-up
  - Write Disable (WRDI) instruction completion
  - Write Status Register (WRSR) instruction completion
  - Write (WRITE) instruction completion
- The Block Protect (BP1, BP0) bits in the Status Register allow part of the memory to be configured as read-only.
- The Write Protect ($\overline{W}$) signal is used to protect the Block Protect (BP1, BP0) bits of the Status Register.

For any instruction to be accepted, and executed, Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) for the last bit of the instruction, and before the next rising edge of Serial Clock (C).

Two points need to be noted in the previous sentence:

- The ‘last bit of the instruction’ can be the eighth bit of the instruction code, or the eighth bit of a data byte, depending on the instruction (except for Read Status Register (RDSR) and Read (READ) instructions).
- The ‘next rising edge of Serial Clock (C)’ might (or might not) be the next bus transaction for some other device on the SPI bus.

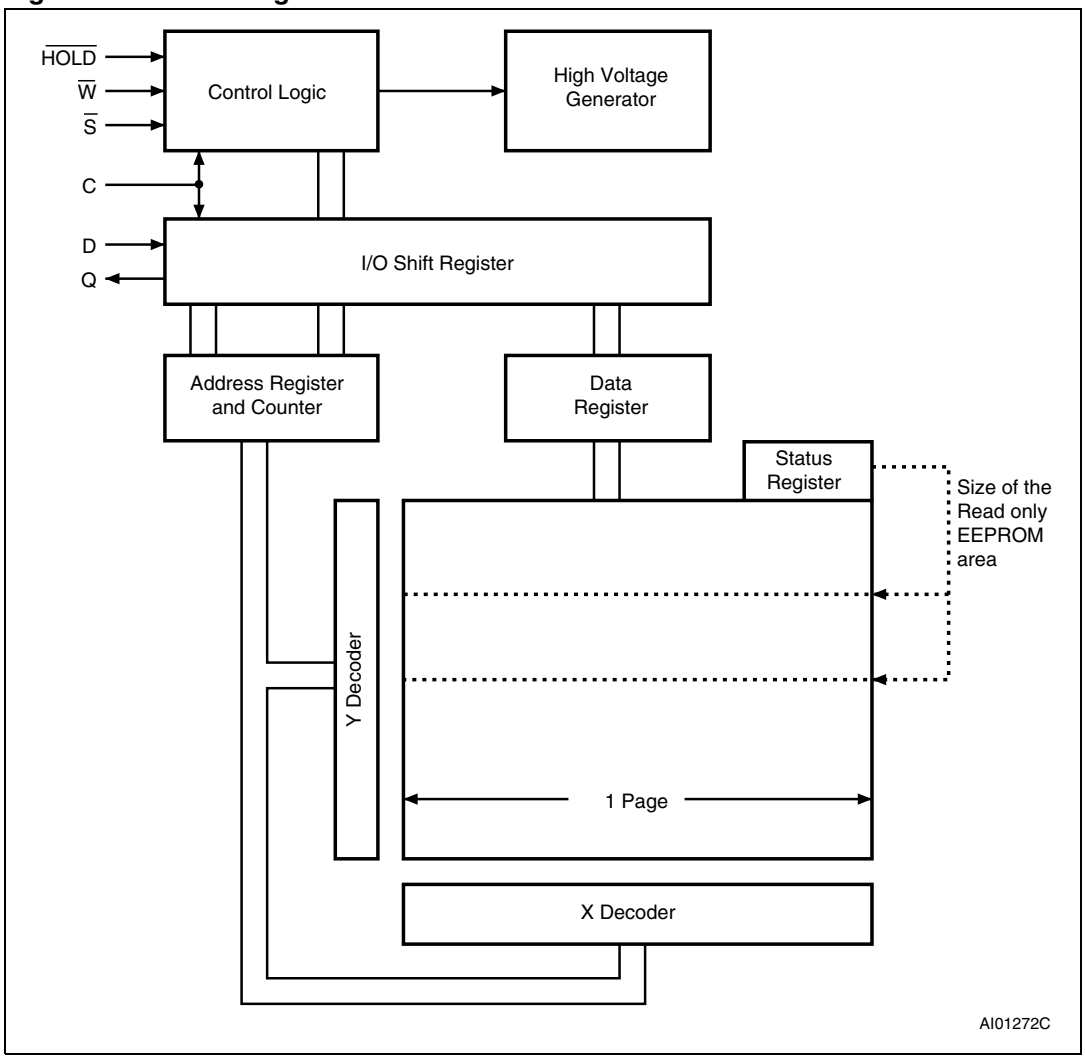
Table 2. Write-protected block size

Status Register bits		Protected block	Array addresses protected
BP1	BP0		64 Kbit devices
0	0	none	none
0	1	Upper quarter	1800h - 1FFFh
1	0	Upper half	1000h - 1FFFh
1	1	Whole memory	0000h - 1FFFh

5 Memory organization

The memory is organized as shown in *Figure 6*.

Figure 6. Block diagram



6 Instructions

Each instruction starts with a single-byte code, as summarized in *Table 3*.

If an invalid instruction is sent (one not contained in <Blue>Table 3.), the device automatically deselects itself.

Table 3. Instruction set

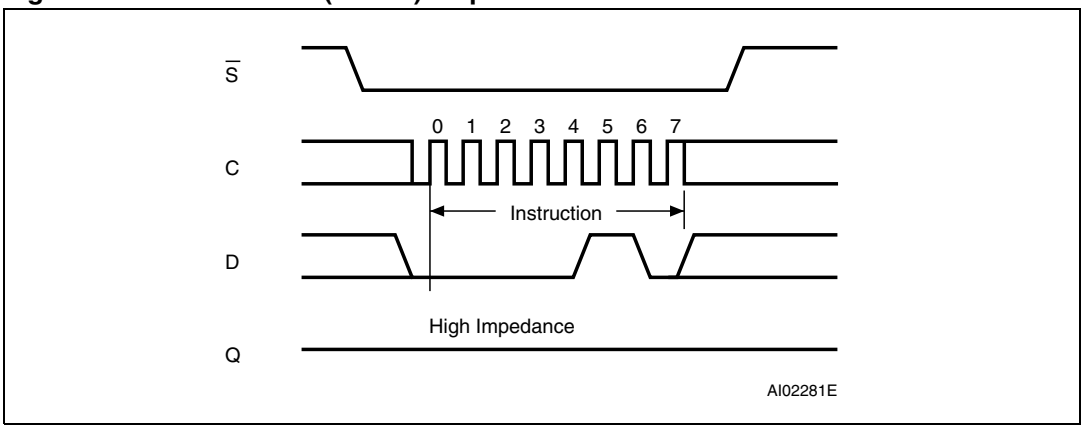
Instruction	Description	Instruction format
WREN	Write Enable	0000 0110
WRDI	Write Disable	0000 0100
RDSR	Read Status Register	0000 0101
WRSR	Write Status Register	0000 0001
READ	Read from Memory Array	0000 0011
WRITE	Write to Memory Array	0000 0010

6.1 Write Enable (WREN)

The Write Enable Latch (WEL) bit must be set prior to each WRITE and WRSR instruction. The only way to do this is to send a Write Enable instruction to the device.

As shown in *Figure 7*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D). The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

Figure 7. Write Enable (WREN) sequence



6.2 Write Disable (WRDI)

One way of resetting the Write Enable Latch (WEL) bit is to send a Write Disable instruction to the device.

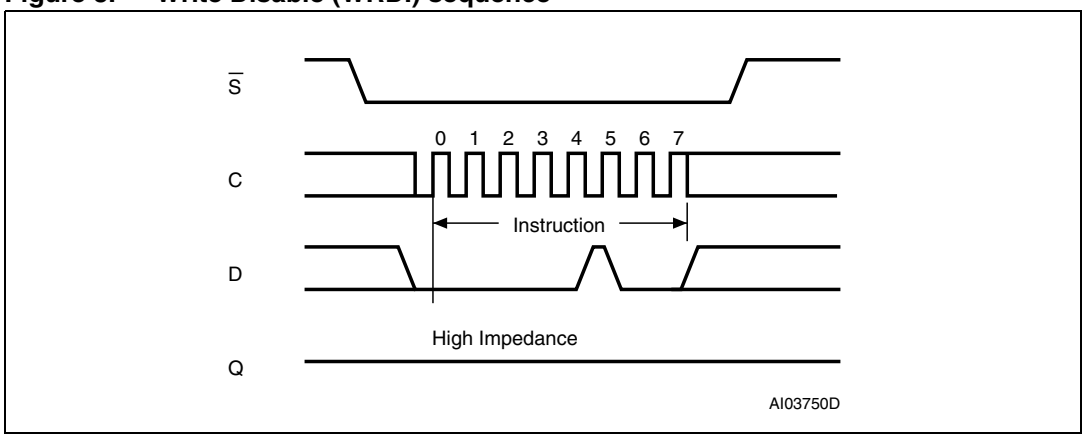
As shown in *Figure 8*, to send this instruction to the device, Chip Select ($\overline{S}$) is driven low, and the bits of the instruction byte are shifted in, on Serial Data Input (D).

The device then enters a wait state. It waits for a the device to be deselected, by Chip Select ($\overline{S}$) being driven high.

The Write Enable Latch (WEL) bit, in fact, becomes reset by any of the following events:

- Power-up
- WRDI instruction execution
- WRSR instruction completion
- WRITE instruction completion.

Figure 8. Write Disable (WRDI) sequence



6.3 Read Status Register (RDSR)

The Read Status Register (RDSR) instruction allows the Status Register to be read. The Status Register may be read at any time, even while a Write or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new instruction to the device. It is also possible to read the Status Register continuously, as shown in *Figure 9*.

The Status Register format is shown in *Table 4* and the status and control bits of the Status Register are as follows:

6.3.1 WIP bit

The Write In Progress (WIP) bit indicates whether the memory is busy with a Write or Write Status Register cycle. When set to 1, such a cycle is in progress, when reset to 0 no such cycle is in progress.

6.3.2 WEL bit

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write or Write Status Register instruction is accepted.

6.3.3 BP1, BP0 bits

The Block Protect (BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Write instructions. These bits are written with the Write Status Register (WRSR) instruction. When one or both of the Block Protect (BP1, BP0) bits is set to 1, the relevant memory area (as defined in *Table 4*) becomes protected against Write (WRITE) instructions. The Block Protect (BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

6.3.4 SRWD bit

The Status Register Write Disable (SRWD) bit is operated in conjunction with the Write Protect ($\overline{W}$) signal. The Status Register Write Disable (SRWD) bit and Write Protect ($\overline{W}$) signal allow the device to be put in the Hardware Protected mode (when the Status Register Write Disable (SRWD) bit is set to 1, and Write Protect ($\overline{W}$) is driven low). In this mode, the non-volatile bits of the Status Register (SRWD, BP1, BP0) become read-only bits and the Write Status Register (WRSR) instruction is no longer accepted for execution.

Table 4. Status Register format

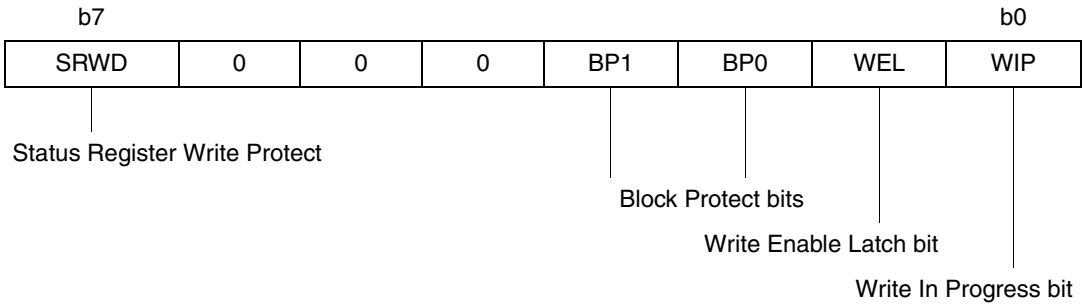
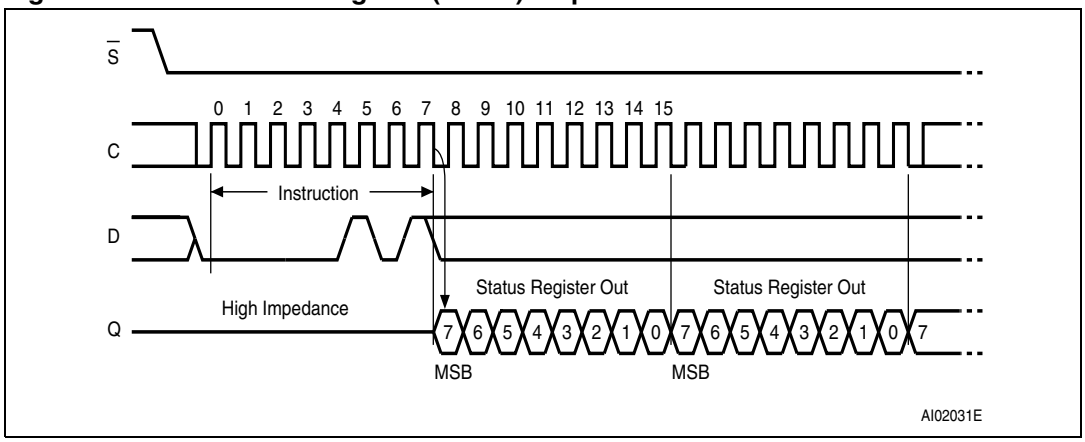


Figure 9. Read Status Register (RDSR) sequence



6.4 Write Status Register (WRSR)

The Write Status Register (WRSR) instruction allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) instruction must previously have been executed.

The Write Status Register (WRSR) instruction is entered by driving Chip Select ($\overline{S}$) low, sending the instruction code followed by the data byte on Serial Data input (D), and driving the Chip Select ($\overline{S}$) signal high. Chip Select ($\overline{S}$) must be driven high after the rising edge of Serial Clock (C) that latches in the eighth bit of the data byte, and before the next rising edge of Serial Clock (C). Otherwise, the Write Status Register (WRSR) instruction is not executed.

Driving the Chip Select ($\overline{S}$) signal high at a byte boundary of the input data triggers the self-timed write cycle that takes t_W to complete (as specified in *Table 17*, *Table 18*, *Table 19* and *Table 20*). The instruction sequence is shown in *Figure 10*.

While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write in progress (WIP) bit: the WIP bit is 1 during the self-timed write cycle t_W, and is 0 when the write cycle is complete. The WEL bit (Write enable latch) is also reset at the end of the write cycle t_W.

The Write Status Register (WRSR) instruction allows the user to change the values of the BP1, BP0 bits and the SRWD bit:

- The Block protect (BP1, BP0) bits define the size of the area that is to be treated as read only, as defined in *Table 2*.
- The SRWD bit (Status register write disable bit), in accordance with the signal read on the Write protect pin ($\overline{W}$), allows the user to set or reset the write protection mode of the Status Register itself, as shown in *Table 5*. When in the Write-protected mode, the Write Status Register (WRSR) instruction is not executed.

The contents of the SRWD and BP1, BP0 bits are updated after the completion of the WRSR instruction, including the t_W write cycle.

The Write Status Register (WRSR) instruction has no effect on the b6, b5, b4, b1 and b0 bits in the Status Register. Bits b6, b5, b4 are always read as 0.

Table 5. Protection modes

$\overline{W}$ signal	SRWD bit	Mode	Write protection of the Status Register	Memory content	
				Protected area(1)	Unprotected area(1)
1	0	Software protected (SPM)	Status Register is Writable (if the WREN instruction has set the WEL bit) The values in the BP1 and BP0 bits can be changed	Write Protected	Ready to accept Write instructions
0	0				
1	1				
0	1	Hardware protected (HPM)	Status Register is Hardware write protected The values in the BP1 and BP0 bits cannot be changed	Write Protected	Ready to accept Write instructions

1. As defined by the values in the Block Protect (BP1, BP0) bits of the Status Register, as shown in *Table 2*.

The protection features of the device are summarized in *Table 5*.

When the Status Register Write Disable (SRWD) bit of the Status Register is 0 (its initial delivery state), it is possible to write to the Status Register provided that the Write Enable Latch (WEL) bit has previously been set by a Write Enable (WREN) instruction, regardless of whether Write Protect ($\overline{W}$) is driven high or low.

When the Status Register Write Disable (SRWD) bit of the Status Register is set to 1, two cases need to be considered, depending on the state of Write Protect ($\overline{W}$):

- If Write Protect ($\overline{W}$) is driven high, it is possible to write to the Status Register provided that the Write enable latch (WEL) bit has previously been set by a Write Enable (WREN) instruction.
- If Write Protect ($\overline{W}$) is driven low, it is *not* possible to write to the Status Register *even* if the Write Enable latch (WEL) bit has previously been set by a Write Enable (WREN) instruction. (Attempts to write to the Status Register are rejected, and are not accepted for execution). As a consequence, all the data bytes in the memory area that are software-protected (SPM) by the Block protect (BP1, BP0) bits in the Status Register, are also hardware-protected against data modification.

Regardless of the order of the two events, the Hardware-protected mode (HPM) can be entered:

- by setting the Status register write disable (SRWD) bit after driving Write Protect ($\overline{W}$) low
- or by driving Write Protect ($\overline{W}$) low after setting the Status register write disable (SRWD) bit.

The only way to exit the Hardware-protected mode (HPM) once entered is to pull Write Protect ($\overline{W}$) high.

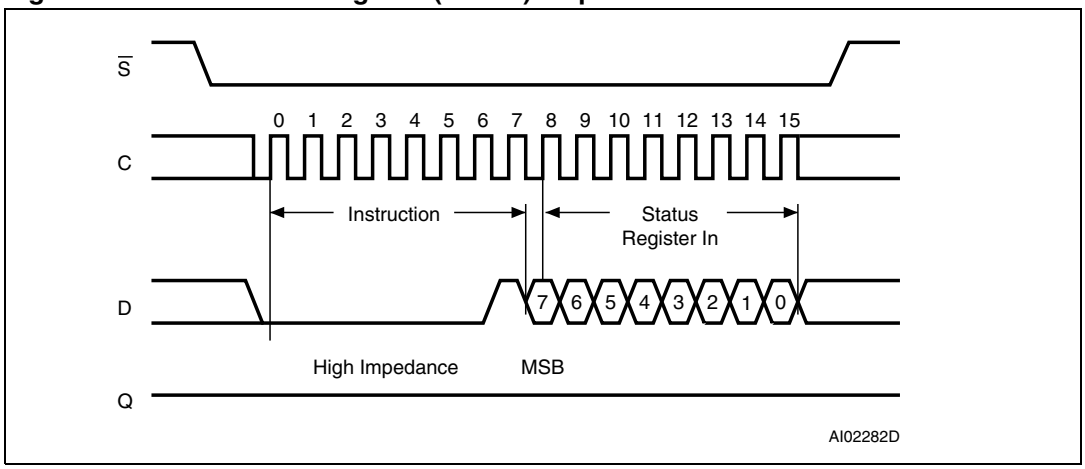
If Write Protect ($\overline{W}$) is permanently tied high, the Hardware-protected mode (HPM) can never be activated, and only the Software-protected mode (SPM), using the Block protect (BP1, BP0) bits in the Status Register, can be used.

Table 6. Address range bits(1)

Device	64 Kbit devices
Address bits	A12-A0

1. b15 to b13 are Don't Care.

Figure 10. Write Status Register (WRSR) sequence



6.5 Read from Memory Array (READ)

As shown in *Figure 11*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte and address bytes are then shifted in, on Serial Data Input (D). The address is loaded into an internal address register, and the byte of data at that address is shifted out, on Serial Data Output (Q).

If Chip Select ($\overline{S}$) continues to be driven low, the internal address register is automatically incremented, and the byte of data at the new address is shifted out.

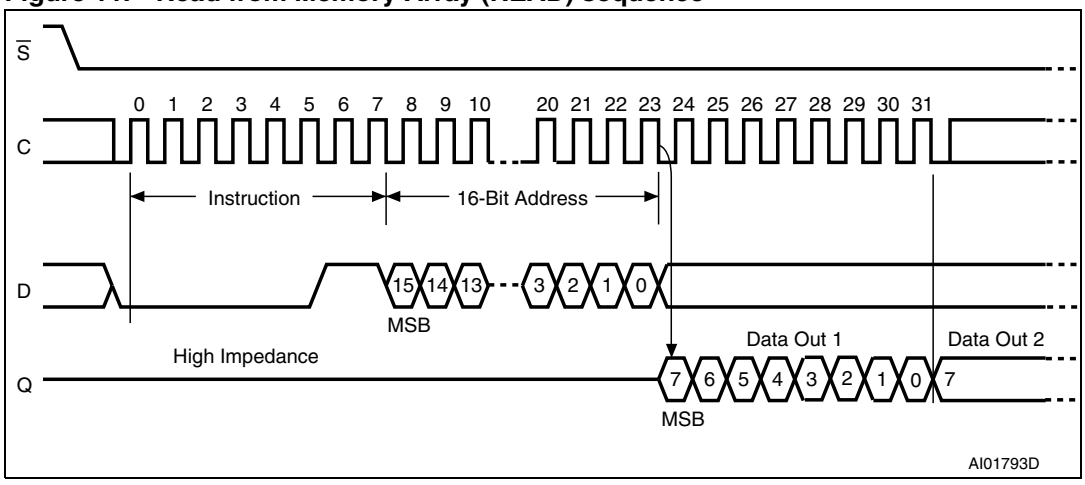
When the highest address is reached, the address counter rolls over to zero, allowing the Read cycle to be continued indefinitely. The whole memory can, therefore, be read with a single READ instruction.

The Read cycle is terminated by driving Chip Select ($\overline{S}$) high. The rising edge of the Chip Select ($\overline{S}$) signal can occur at any time during the cycle.

The first byte addressed can be any byte within any page.

The instruction is not accepted, and is not executed, if a Write cycle is currently in progress.

Figure 11. Read from Memory Array (READ) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

6.6 Write to Memory Array (WRITE)

As shown in *Figure 12*, to send this instruction to the device, Chip Select ($\overline{S}$) is first driven low. The bits of the instruction byte, address byte, and at least one data byte are then shifted in, on Serial Data Input (D).

The instruction is terminated by driving Chip Select ($\overline{S}$) high at a byte boundary of the input data. In the case of *Figure 12*, this occurs after the eighth bit of the data byte has been latched in, indicating that the instruction is being used to write a single byte. The self-timed Write cycle starts from the rising edge of Chip Select ($\overline{S}$), and continues for a period t_{WC} (as specified in *Table 18* to *Table 20*), at the end of which the Write in Progress (WIP) bit is reset to 0.

If, though, Chip Select ($\overline{S}$) continues to be driven low, as shown in *Figure 13*, the next byte of input data is shifted in, so that more than a single byte, starting from the given address towards the end of the same page, can be written in a single internal Write cycle.

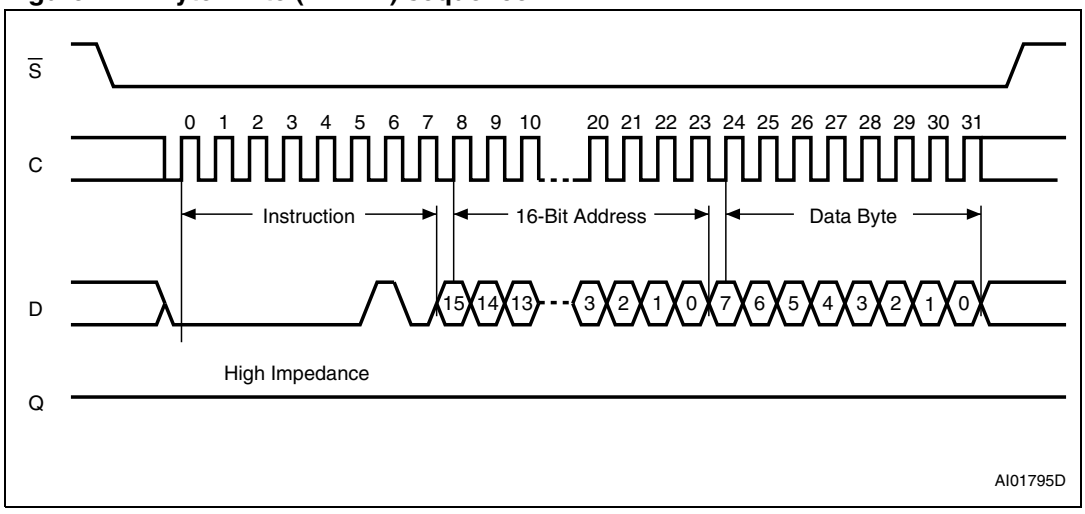
Each time a new data byte is shifted in, the least significant bits of the internal address counter are incremented. If the number of data bytes sent to the device exceeds the page boundary, the internal address counter rolls over to the beginning of the page, and the previous data there are overwritten with the incoming data. (The page size of these devices is 32 bytes).

The instruction is not accepted, and is not executed, under the following conditions:

- if the Write Enable Latch (WEL) bit has not been set to 1 (by executing a Write Enable instruction just before)
- if a write cycle is already in progress
- if the device has not been deselected, by Chip Select ($\overline{S}$) being driven high, at a byte boundary (after the eighth bit, b0, of the last data byte that has been latched in)
- if the addressed page is in the region protected by the Block Protect (BP1 and BP0) bits.

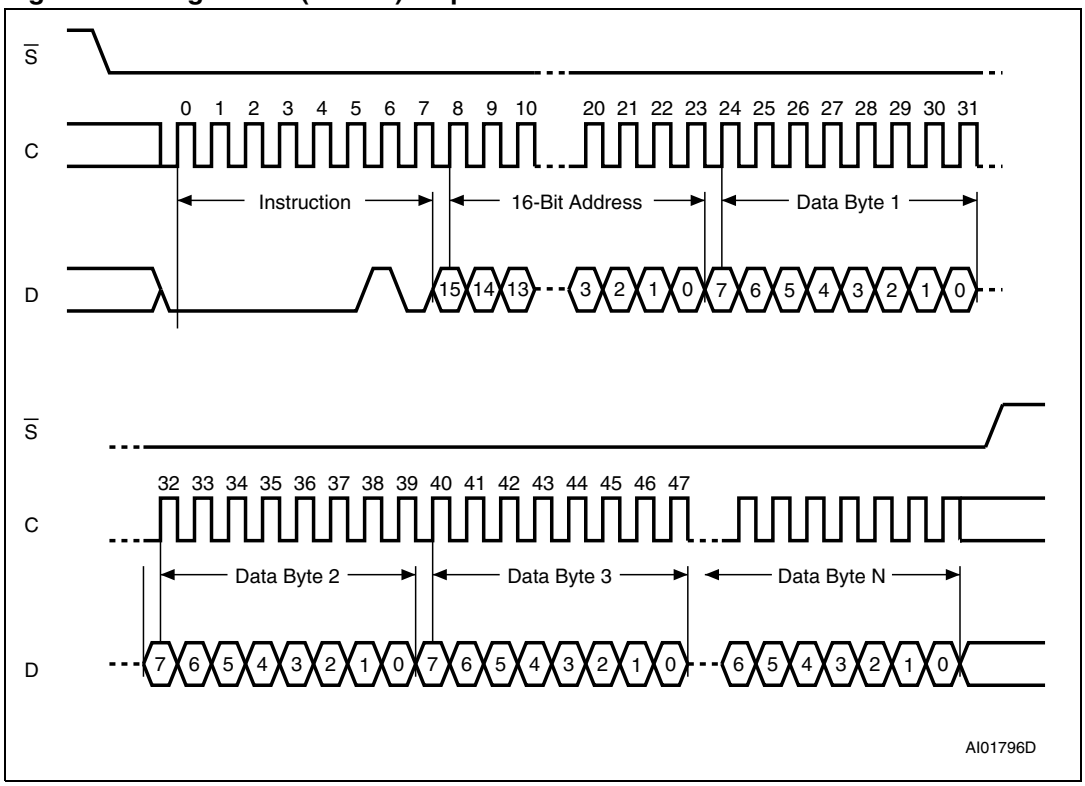
Note: The self-timed write cycle t_W is internally executed as a sequence of two consecutive events: [Erase addressed byte(s)], followed by [Program addressed byte(s)]. An erased bit is read as "0" and a programmed bit is read as "1".

Figure 12. Byte Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

Figure 13. Page Write (WRITE) sequence



1. Depending on the memory size, as shown in *Table 6*, the most significant address bits are Don't Care.

7 Power-up and delivery state

7.1 Power-up state

After Power-up, the device is in the following state:

- Standby Power mode
- deselected (after power-up, a falling edge is required on Chip Select ($\overline{S}$) before any instructions can be started).
- not in the Hold condition
- the Write Enable Latch (WEL) is reset to 0
- Write In Progress (WIP) is reset to 0

The SRWD, BP1 and BP0 bits of the Status Register are unchanged from the previous power-down (they are non-volatile bits).

7.2 Initial delivery state

The device is delivered with the memory array set to all 1s (each byte = FFh). The Status register write disable (SRWD) and Block protect (BP1 and BP0) bits are initialized to 0.

8 Maximum rating

Stressing the device outside the ratings listed in *Table 7* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 7. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	150	°C
T_A	Ambient operating temperature	–40	130	°C
T_{LEAD}	Lead temperature during soldering	See note (1)		°C
V_O	Output voltage	–0.50	V_{CC}+0.6	V
V_I	Input voltage	–0.50	6.5	V
I_{OL}	DC output current (Q = 0)		5	mA
I_{OH}	DC output current (Q = 1)		–5	mA
V_{CC}	Supply voltage	–0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (human body model)(2)	–4000	4000	V

1. Compliant with JEDEC Std J-STD-020C (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU
2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114, C1 = 100 pF, R1 = 1500 Ω, R2 = 500 Ω)

9 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 8. Operating conditions (M95640)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	4.5	5.5	V
T_A	Ambient operating temperature (device grade 3)	–40	125	°C

Table 9. Operating conditions (M95640-W)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	2.5	5.5	V
T_A	Ambient operating temperature (device grade 6)	–40	85	°C
	Ambient operating temperature (device grade 3)	–40	125	°C

Table 10. Operating conditions (M95640-R)

Symbol	Parameter	Min.(1)	Max. (1)	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

1. This product is under development. For more information, please contact your nearest ST sales office.

Table 11. AC measurement conditions(1)

Symbol	Parameter	Min.	Typ.	Max.	Unit
C_L	Load capacitance		30		pF
	Input rise and fall times			50	ns
	Input pulse voltages	$0.2V_{CC}$ to $0.8V_{CC}$			V
	Input and output timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$			V

1. Output Hi-Z is defined as the point where data out is no longer driven.

Figure 14. AC measurement I/O waveform

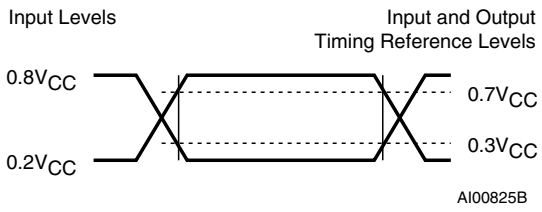


Table 12. Capacitance(1)

Symbol	Parameter	Test condition	Min.	Max.	Unit
C_{OUT}	Output capacitance (Q)	V_{OUT} = 0 V		8	pF
C_{IN}	Input capacitance (D)	V_{IN} = 0 V		8	pF
	Input capacitance (other pins)	V_{IN} = 0 V		6	pF

1. Sampled only, not 100% tested.

Table 13. DC characteristics (M95640, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 5V, Q = open		4	mA
		C = 0.1V_{CC}/0.9V_{CC} at 10 MHz, V_{CC} = 5V, Q = open		8	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 5 V, $V_{IN} = V_{SS}$ or V_{CC}		5	µA
V_{IL}	Input low voltage		–0.45	0.3 V_{CC}	V
V_{IH}	Input high voltage		0.7 V_{CC}	V_{CC}+1	V
V_{OL}(1)	Output low voltage	I_{OL} = 2 mA, V_{CC} = 5 V		0.4	V
V_{OH}(1)	Output high voltage	I_{OH} = –2 mA, V_{CC} = 5 V	0.8 V_{CC}		V
V_{RES}(2)	Internal reset threshold voltage		2.5	4.0	V

1. For all 5 V range devices, the device meets the output requirements for both TTL and CMOS standards.
2. Characterized only, not 100% tested.

Table 14. DC characteristics (M95640-W, device grade 6)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		3	mA
		C = 0.1V_{CC}/0.9V_{CC} at 10 MHz, V_{CC} = 3.0 V, Q = open		4	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 2.5 V $V_{IN} = V_{SS}$ or V_{CC}		1	µA
		$\overline{S} = V_{CC}$, V_{CC} = 5.0 V $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V or I_{OL} = 2 mA, V_{CC} = 5.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V or I_{OH} = –2 mA, V_{CC} = 5.5 V	0.8V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

Table 15. DC characteristics (M95640-W, device grade 3)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, $V_{OUT} = V_{SS}$ or V_{CC}		± 2	µA
I_{CC}	Supply current	C = 0.1V_{CC}/0.9V_{CC} at 5 MHz, V_{CC} = 2.5 V, Q = open		3	mA
		C = 0.1V_{CC}/0.9V_{CC} at 10 MHz, V_{CC} = 2.5 V, Q = open		6	mA
I_{CC1}	Supply current (Standby)	$\overline{S} = V_{CC}$, V_{CC} = 2.5 V, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
V_{IL}	Input low voltage		–0.45	0.3V_{CC}	V
V_{IH}	Input high voltage		0.7V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	I_{OL} = 1.5 mA, V_{CC} = 2.5 V		0.4	V
V_{OH}	Output high voltage	I_{OH} = –0.4 mA, V_{CC} = 2.5 V	0.8V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

Table 16. DC characteristics (M95640-R)

Symbol	Parameter	Test condition	Min.	Max.	Unit
I_{LI}	Input leakage current	$V_{IN} = V_{SS}$ or V_{CC}		± 2	µA
I_{LO}	Output leakage current	$\overline{S} = V_{CC}$, voltage applied on Q = V_{SS} or V_{CC}		± 2	µA
I_{CCR}	Supply current (Read)	V_{CC} = 2.5 V, C = 0.1V_{CC}/0.9V_{CC} at maximum clock frequency, Q = open		3	mA
		V_{CC} = 1.8 V, C = 0.1V_{CC}/0.9V_{CC} at maximum clock frequency, Q = open		2	mA
I_{CC1}	Supply current (Standby)	V_{CC} = 5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		2	µA
		V_{CC} = 2.5 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1	µA
		V_{CC} = 1.8 V, $\overline{S} = V_{CC}$, $V_{IN} = V_{SS}$ or V_{CC}		1	µA
V_{IL}	Input low voltage	1.8 V < V_{CC} < 2.5 V	–0.45	0.25V_{CC}	V
		2.5 V < V_{CC} < 5.5 V	–0.45	0.3V_{CC}	V
V_{IH}	Input high voltage	1.8 V < V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
		2.5 V < V_{CC} < 5.5 V	0.7 V_{CC}	V_{CC}+1	V
V_{OL}	Output low voltage	V_{CC} = 2.5 V, I_{OL} = 1.5 mA or V_{CC} = 5.5 V, I_{OL} = 2 mA		0.2V_{CC}	V
		V_{CC} = 1.8 V, I_{OL} = 0.15 mA		0.3	V
V_{OH}	Output high voltage	V_{CC} = 2.5 V, I_{OH} = –0.4 mA or V_{CC} = 5.5 V, I_{OH} = –2 mA or V_{CC} = 1.8 V, I_{OH} = –0.1 mA	0.8 V_{CC}		V
V_{RES}(1)	Internal reset threshold voltage		1.0	1.65	V

1. Characterized only, not 100% tested.

Table 17. AC characteristics (M95640, device grade 3)

Test conditions specified in *Table 10* and *Table 11*							
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Min.(1)**	**Max.(1)**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	5	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		30		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		30		ns
t_{CH}(2)	t_{CLH}	Clock high time	90		42		ns
t_{CL}(2)	t_{CLL}	Clock low time	90		40		ns
t_{CLCH}(3)	t_{RC}	Clock rise time		1		2	µs
t_{CHCL}(3)	t_{FC}	Clock fall time		1		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		10		ns
t_{CHDX}	t_{DH}	Data in hold time	30		10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		30		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0		ns
t_{SHQZ}(3)	t_{DIS}	Output disable time		100		40	ns
t_{CLQV}(4)	t_V	Clock low to output valid		60		40	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		ns
t_{QLQH}(3)	t_{RO}	Output rise time		50		40	ns
t_{QHQL}(3)	t_{FO}	Output fall time		50		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50		40	ns
t_{HLQZ}(3)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100		40	ns
t_W	t_{WC}	Write time		5		5	ms

1. These timings are offered with grade3 devices referenced with “/PC” process letters only (see the last digits in the *Part numbering*).
2. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
3. Value guaranteed by characterization, not 100% tested in production.
4. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a Read setup time t_{SU} = 0 ns, t_{CL} can be equal to (or greater than) t_{CLQV}; in all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.

Table 18. AC characteristics (M95640-W, device grade 6)

Test conditions specified in *Table 9* and *Table 11*					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	30		ns
t_{CHSL}		$\overline{S}$ not active hold time	30		ns
t_{CH}(1)	t_{CLH}	Clock high time	42		ns
t_{CL}(1)	t_{CLL}	Clock low time	40		ns
t_{CLCH}(2)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	10		ns
t_{CHDX}	t_{DH}	Data in hold time	10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	30		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		ns
t_{SHQZ}(2)	t_{DIS}	Output disable time		40	ns
t_{CLQV}(3)	t_V	Clock low to output valid		40	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		40	ns
t_{QHQL}(2)	t_{FO}	Output fall time		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		40	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		40	ns
t_W	t_{WC}	Write time		5	ms

1. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
2. Value guaranteed by characterization, not 100% tested in production.
3. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a Read setup time $t_{SU} = 0$ ns, t_{CL} can be equal to (or greater than) t_{CLQV}; in all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.

Table 19. AC characteristics (M95640-W, device grade 3)

Test conditions specified in *Table 9* and *Table 11*							
Symbol	Alt.	Parameter	2.5 V to 5.5 V		3.0 V to 5.5 V(1)		Unit
			Min.	Max.	Min.	Max.	
f_C	f_{SCK}	Clock frequency	D.C.	5	D.C.	10	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	90		30		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	90		30		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	100		40		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	90		30		ns
t_{CHSL}		$\overline{S}$ not active hold time	90		30		ns
t_{CH}(2)	t_{CLH}	Clock high time	90		42		ns
t_{CL}(2)	t_{CLL}	Clock low time	90		40		ns
t_{CLCH}(3)	t_{RC}	Clock rise time		1		2	µs
t_{CHCL}(3)	t_{FC}	Clock fall time		1		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	20		10		ns
t_{CHDX}	t_{DH}	Data in hold time	30		10		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	70		30		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	40		30		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0		ns
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0		ns
t_{SHQZ}(3)	t_{DIS}	Output disable time		100		40	ns
t_{CLQV}(4)	t_V	Clock low to output valid		60		40	ns
t_{CLQX}	t_{HO}	Output hold time	0		0		ns
t_{QLQH}(3)	t_{RO}	Output rise time		50		40	ns
t_{QHQL}(3)	t_{FO}	Output fall time		50		40	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		50		40	ns
t_{HLQZ}(3)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		100		40	ns
t_W	t_{WC}	Write time		5		5	ms

1. These timings are offered with grade3 devices referenced with “/PC” process letters only (see the last digits in the *Part numbering*).
2. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
3. Value guaranteed by characterization, not 100% tested in production.
4. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a Read setup time t_{SU} = 0 ns, t_{CL} can be equal to (or greater than) t_{CLQV}; in all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.

Table 20. AC characteristics (M95640-R)

Test conditions specified in *Table 10* and *Table 11*(1)					
Symbol	**Alt.**	**Parameter**	**Min.**	**Max.**	**Unit**
f_C	f_{SCK}	Clock frequency	D.C.	2	MHz
t_{SLCH}	t_{CSS1}	$\overline{S}$ active setup time	150		ns
t_{SHCH}	t_{CSS2}	$\overline{S}$ not active setup time	150		ns
t_{SHSL}	t_{CS}	$\overline{S}$ deselect time	200		ns
t_{CHSH}	t_{CSH}	$\overline{S}$ active hold time	150		ns
t_{CHSL}		$\overline{S}$ not active hold time	150		ns
t_{CH}(2)	t_{CLH}	Clock high time	200		ns
t_{CL}(1)	t_{CLL}	Clock low time	200		ns
t_{CLCH}(3)	t_{RC}	Clock rise time		2	µs
t_{CHCL}(2)	t_{FC}	Clock fall time		2	µs
t_{DVCH}	t_{DSU}	Data in setup time	50		ns
t_{CHDX}	t_{DH}	Data in hold time	50		ns
t_{HHCH}		Clock low hold time after $\overline{HOLD}$ not active	150		ns
t_{HLCH}		Clock low hold time after $\overline{HOLD}$ active	150		ns
t_{CLHL}		Clock low set-up time before $\overline{HOLD}$ active	0		0
t_{CLHH}		Clock low set-up time before $\overline{HOLD}$ not active	0		0
t_{SHQZ}(2)	t_{DIS}	Output disable time		200	ns
t_{CLQV}(4)	t_V	Clock low to output valid		200	ns
t_{CLQX}	t_{HO}	Output hold time	0		ns
t_{QLQH}(2)	t_{RO}	Output rise time		200	ns
t_{QHQL}(2)	t_{FO}	Output fall time		200	ns
t_{HHQV}	t_{LZ}	$\overline{HOLD}$ high to output valid		200	ns
t_{HLQZ}(2)	t_{HZ}	$\overline{HOLD}$ low to output high-Z		200	ns
t_W	t_{WC}	Write time		5	ms

1. If the application uses the M95640-R device with 2.5 V ≤ V_{CC} ≤ 5.5 V and –40 °C ≤ T_A ≤ +85 °C, please refer to *Table 18: AC characteristics (M95640-W, device grade 6)* instead of the above table.
2. $t_{CH} + t_{CL}$ must never be lower than the shortest possible clock period, $1/f_C$(max).
3. Value guaranteed by characterization, not 100% tested in production.
4. t_{CLQV} must be compatible with t_{CL} (clock low time): if the SPI bus master offers a Read setup time t_{SU} = 0 ns, t_{CL} can be equal to (or greater than) t_{CLQV}; in all other cases, t_{CL} must be equal to (or greater than) $t_{CLQV}+t_{SU}$.

Figure 15. Serial input timing

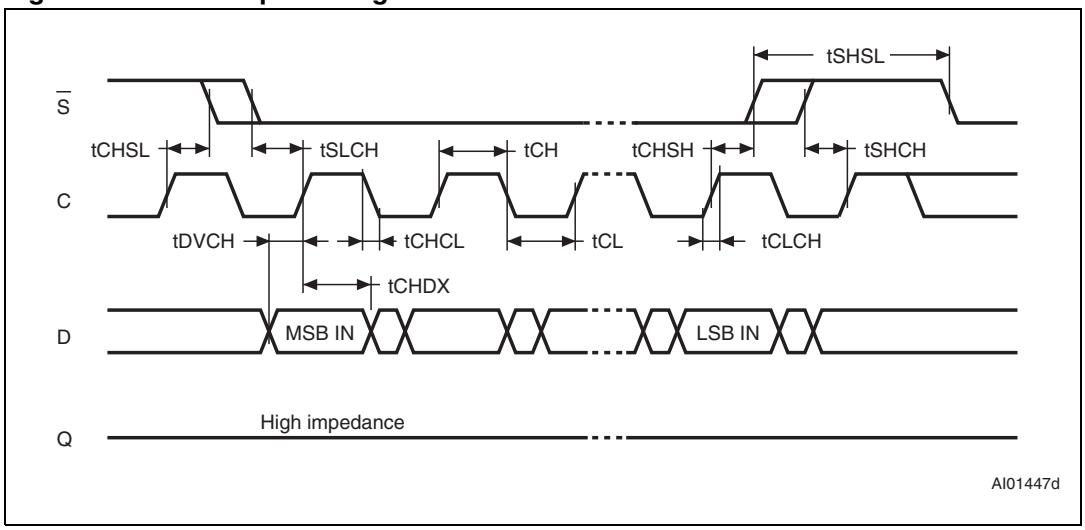


Figure 16. Hold timing

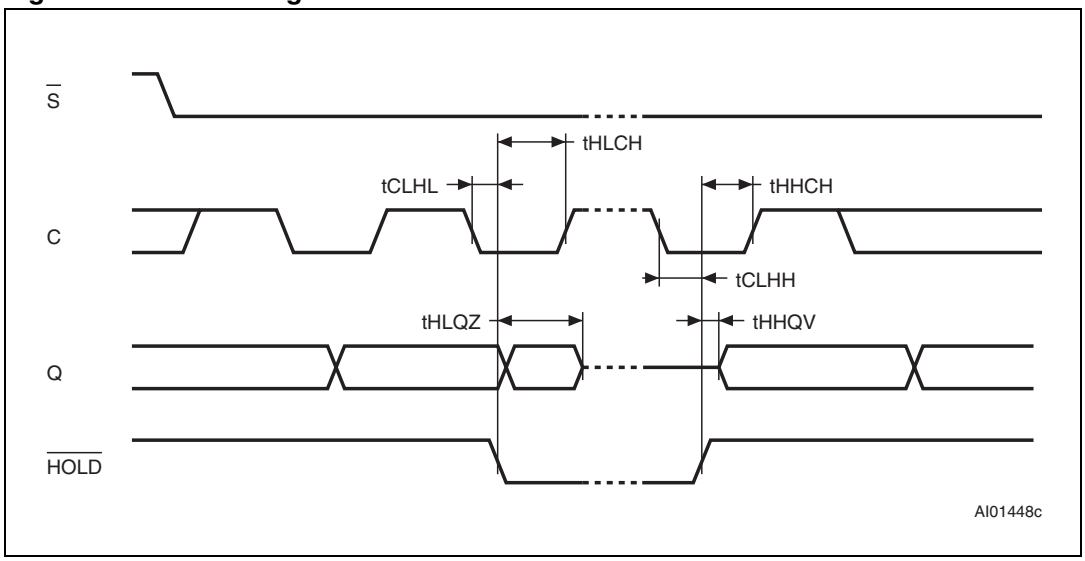
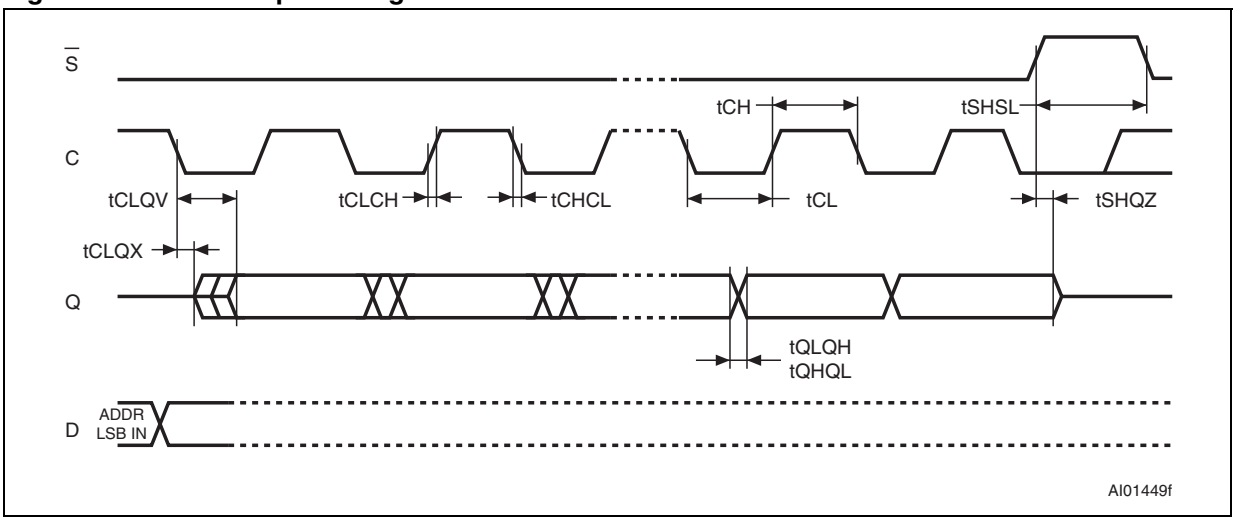


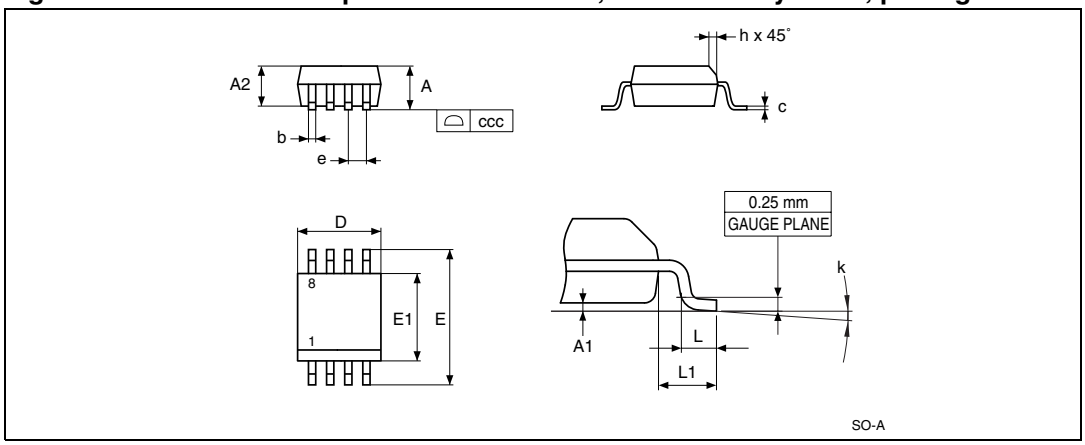
Figure 17. Serial output timing



10 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 18. SO8N – 8-lead plastic small outline, 150 mils body width, package outline



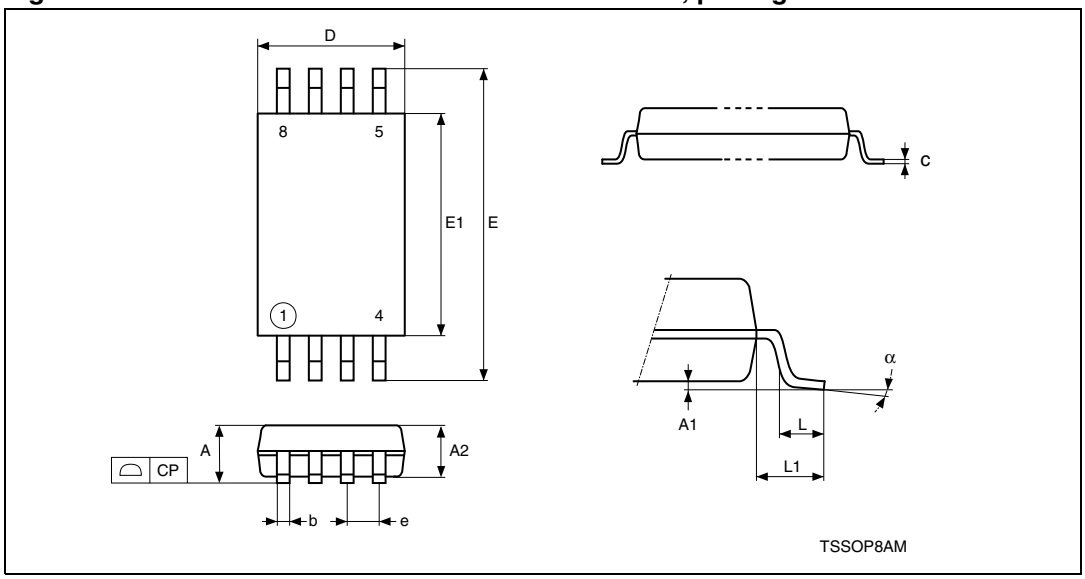
1. Drawing is not to scale.

Table 21. SO8N – 8-lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.10	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.10			0.0039
D	4.90	4.80	5.00	0.1929	0.189	0.1969
E	6.00	5.80	6.20	0.2362	0.2283	0.2441
E1	3.90	3.80	4.00	0.1535	0.1496	0.1575
e	1.27	–	–	0.05	-	-
h		0.25	0.50		0.0098	0.0197
k		0°	8°		0°	8°
L		0.40	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 19. TSSOP8 – 8-lead thin shrink small outline, package outline



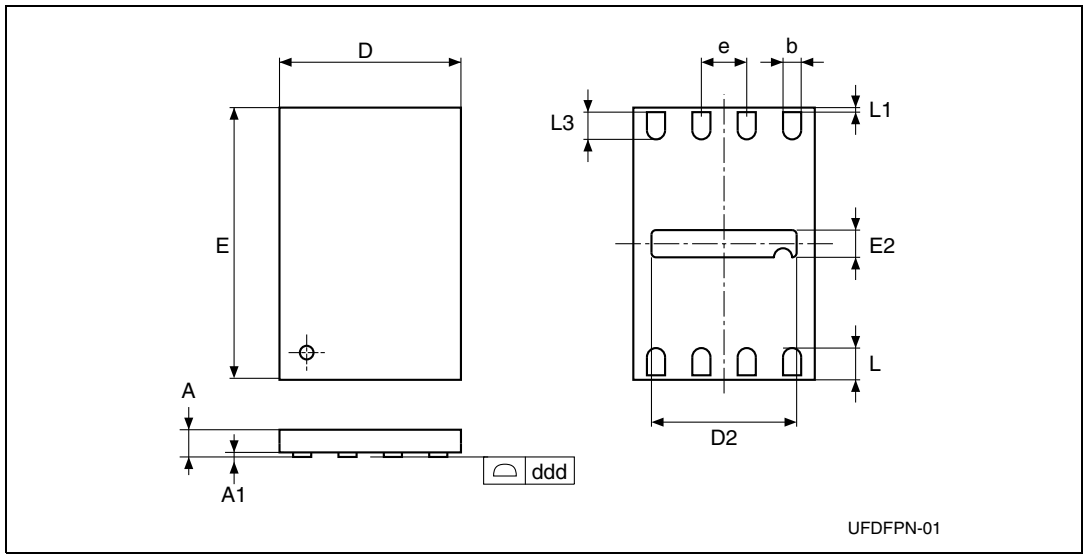
1. Drawing is not to scale.

Table 22. TSSOP8 – 8-lead thin shrink small outline, package mechanical data

Symbol	millimeters			inches[1]		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2	1.000	0.800	1.050	0.0394	0.0315	0.0413
b		0.190	0.300		0.0075	0.0118
c		0.090	0.200		0.0035	0.0079
CP			0.100			0.0039
D	3.000	2.900	3.100	0.1181	0.1142	0.1220
e	0.650	–	–	0.0256	–	–
E	6.400	6.200	6.600	0.2520	0.2441	0.2598
E1	4.400	4.300	4.500	0.1732	0.1693	0.1772
L	0.600	0.450	0.750	0.0236	0.0177	0.0295
L1	1.000			0.0394		
α		0°	8°		0°	8°

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 20. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline



1. Drawing is not to scale.
2. The central pad (the area E2 by D2 in the above illustration) is internally pulled to V_{SS}. It must not be connected to any other voltage or signal line on the PCB, for example during the soldering process.

Table 23. UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A	0.55	0.45	0.6	0.0217	0.0177	0.0236
A1	0.02	0	0.05	0.0008	0	0.002
b	0.25	0.2	0.3	0.0098	0.0079	0.0118
D	2	1.9	2.1	0.0787	0.0748	0.0827
D2	1.6	1.5	1.7	0.063	0.0591	0.0669
E	3	2.9	3.1	0.1181	0.1142	0.122
E2	0.2	0.1	0.3	0.0079	0.0039	0.0118
e	0.5	-	-	0.0197	-	-
L	0.45	0.4	0.5	0.0177	0.0157	0.0197
L1			0.15			0.0059
L3		0.3			0.0118	
ddd[2]	0.08			0.08		

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Applied for exposed die paddle and terminals. Exclude embedding part of exposed die paddle from measurement.

11 Part numbering

Table 24. Ordering information scheme

Example: M95640 – W MN 6 T P /P

Device type

M95 = SPI serial access EEPROM

Device function

640 = 64 Kbit (8192 × 8)

Operating voltage

blank = V_{CC} = 4.5 to 5.5 V

W = V_{CC} = 2.5 to 5.5 V

R = V_{CC} = 1.8 to 5.5 V

Package(1)

MN = SO8 (150 mils width)

DW = TSSOP8 (169 mils width)

MB = MLP8 (2 × 3 mm)

Device grade

6 = Industrial temperature range, –40 to 85 °C.

Device tested with standard test flow

3 = Device tested with high reliability certified flow(2)automotive temperature range (–40 to 125 °C)

Option

blank = Standard packing

T = Tape and reel packing

Plating technology

P or G = ECOPACK (RoHS compliant)

Process letter(3)

/P or /PC = DP26% Chartered

1. All packages are ECOPACK2® (RoHS compliant and Halogen-free).
2. ST strongly recommends the use of the Automotive Grade devices for use in an automotive environment. The high reliability certified flow (HRCF) is described in the quality note QNEE9801. Please ask your nearest ST sales office for a copy.
3. The process letter only concerns Grade-3 devices.

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 25. Available M95640x products (package, voltage range, temperature grade)

Package	M95640 4.5 V to 5.5 V	M95640-W 2.5 V to 5.5 V	M95640-R 1.8 V to 5.5 V
SO8 (MN)	Range 3	Range 6 Range 3	Range 6
TSSOP (DW)	-	Range 6 Range 3	Range 6
MLP 2 × 3 mm (MB)	-	-	Range 6

12 Revision history

Table 26. Document revision history

Date	Revision	Changes
13-Jul-2000	1.2	Human Body Model meets JEDEC std (Table 2). Minor adjustments on pp 1,11,15. New clause on p7. Addition of TSSOP8 package on pp 1, 2, Ordering Info, Mechanical Data
16-Mar-2001	1.3	Test condition added I_{LI} and I_{LO}, and specification of t_{DLDH} and t_{DHDL} removed. t_{CLCH}, t_{CHCL}, t_{DLDH} and t_{DHDL} changed to 50ns for the -V range. “-V” Voltage range changed to “2.7V to 3.6V” throughout. Maximum lead soldering time and temperature conditions updated. Instruction sequence illustrations updated. “Bus Master and Memory Devices on the SPI bus” illustration updated. Package Mechanical data updated
19-Jul-2001	1.4	M95160 and M95080 devices removed to their own data sheet
06-Dec-2001	1.5	Endurance increased to 1M write/erase cycles Instruction sequence illustrations updated
18-Dec-2001	2.0	Document reformatted using the new template. No parameters changed.
08-Feb-2002	2.1	Announcement made of planned upgrade to 10MHz clock for the 5V, –40 to 85°C, range. Endurance set to 100K write/erase cycles
18-Dec-2002	2.2	10MHz, 5MHz, 2MHz clock; 5ms, 10ms Write Time; 100K, 1M erase/write cycles distinguished on front page, and in the DC and AC Characteristics tables
26-Mar-2003	2.3	Process identification letter corrected in footnote to AC Characteristics table for temp. range 3
26-Jun-2003	2.4	-S voltage range upgraded by removing it and inserting -R voltage range in its place
15-Oct-2003	3.0	Table of contents, and Pb-free options added. V_{IL}(min) improved to -0.45V
21-Nov-2003	3.1	V_I(min) and V_O(min) corrected (improved) to -0.45V
28-Jan-2004	4.0	TSSOP8 connections added to DIP and SO connections
24-May-2005	5.0	M95320-S and M95640-S root part numbers (1.65 to 5.5V Supply) and related characteristics added. 20MHz Clock rate added.TSSOP14 package removed and MLP8 package added. Description of *Power On Reset: VCC Lock-Out Write Protect* updated. Product List summary table added. Absolute Maximum Ratings for V_{IO}(min) and V_{CC}(min) improved. Soldering temperature information clarified for RoHS compliant devices. Device Grade 3 clarified, with reference to HRCF and automotive environments. AEC-Q100-002 compliance. t_{CHHL}(min) and t_{CHHH}(min) is t_{CH} for products under “S” process. t_{HHQX} corrected to t_{HHQV}. *Figure 16: Hold timing* updated.

Table 26. Document revision history (continued)

Date	Revision	Changes
07-Jul-2006	6	Document converted to new ST template. Packages are ECOPACK® compliant. PDIP package removed. SO8N package specifications updated (see *Table 21* and *Figure 18*). M95640-S and M95320-S part numbers removed (*DC and AC parameters* updated accordingly). *How to identify previous, current and new products by the Process identification letter* Table removed. *Figure 4: SPI modes supported* updated and *Note 2* added. First three paragraphs of *Section 4: Operating features* replaced by *Section 4.1: Supply voltage (V_{CC})*. T_A added to *Table 7: Absolute maximum ratings*. I_{CC} and I_{CC1} updated in *Table 13*, *Table 13*, *Table 14* and *Table 16*. V_{OL} and V_{OH} updated in *Table 14*. I_{CC} updated in *Table 15*. Data in *Table 16* is no longer preliminary. t_{CH} updated in *Table 18*. *Table 21: AC characteristics (M95640-R)* added. Timing line of t_{SHQZ} modified in *Figure 17: Serial output timing*. *Process letter* added to *Table 24: Ordering information scheme*, Note 2 removed. Note 2 removed from *Figure 2*.
09-Oct-2007	7	JEDEC standard revision updated to D in *Note 1* below *Table 7: Absolute maximum ratings*. Note 2 removed below *Figure 3* and explanatory paragraph added. *Section 4.1: Supply voltage (V_{CC})* updated. *Table 6: Address range bits* corrected. Products operating at V_{CC} = 4.5 V to 5.5 V are no longer available in the device grade 6 T_A temperature range. I_{CC} and I_{CC1} parameters modified in *Table 14: DC characteristics (M95640-W, device grade 6)*. Maximum frequency for M95320-W and M95640-W upgraded from 5 MHz to 10 MHz in the device grade 6 T_A temperature range (*Table 18: AC characteristics (M95640-W, device grade 6)* modified accordingly). *Table 27: Available M95640x products (package, voltage range, temperature grade)*: /PB process letter added, /P process letter removed. Blank option removed below Plating technology in *Table 24: Ordering information scheme*. *Table 25* and *Table 27* added. Small text changes. *Table 23: UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package mechanical data* updated. Package mechanical inch values calculated from mm and rounded to 4 decimal digits in *Section 10: Package mechanical data*.
17-Dec-2007	8	*Section 2.7: V_{SS} ground* added. Device behavior when V_{CC} passes over the POR threshold updated (see *Section 4.1.2: Device reset* and *Section 4.1.4: Power-down*). V_{IL} and V_{IH} modified in *Table 16: DC characteristics (M95640-R)*. t_W, write time, modified in *Table 20: AC characteristics (M95320-R)* and *Table 21: AC characteristics (M95640-R)*. Small text changes.

Table 26. Document revision history (continued)

Date	Revision	Changes
20-Mar-2008	9	*Section 4.1: Supply voltage (V_{CC})* updated. 10 MHz frequencies added to *Table 17: AC characteristics (M95640, device grade 3)* and *Table 19: AC characteristics (M95640-W, device grade 3)*. Small text changes.
23-Jun-2008	10	*Section 4.1: Supply voltage (V_{CC})* updated. *Table 16: DC characteristics (M95640-R)* modified. *Figure 15: Serial input timing*, *Figure 16: Hold timing* and *Figure 17: Serial output timing* modified.
17-Feb-2009	11	*Section 4.1: Supply voltage (V_{CC})* and *Section 6.4: Write Status Register (WRSR)* updated. Note added to *Section 6.6: Write to Memory Array (WRITE)*. *Section 7.2: Initial delivery state* specified. Note modified in *Table 12: Capacitance*. I_{CC} at 10 MHz added to *Table 13: DC characteristics (M95640, device grade 3)*. V_{RES} parameter added to DC characteristics tables *13*, *14*, *15* and *16*. Note added to t_{CLQV} in AC characteristics tables *17*, *18*, *19* and *21*. Note added to *Table 20: AC characteristics (M95320-R)* and *Table 21: AC characteristics (M95640-R)*. Process letter modified in *Table 24: Ordering information scheme*.
07-Dec-2009	12	32 Kbit densities removed from datasheet. ECOPACK status of packages specified in *Features* and in *Table 24: Ordering information scheme*. I_{OL} and I_{OH} added to *Table 7: Absolute maximum ratings*. *Note 2* added below *Figure 20: UFDFPN8 (MLP8) - 8-lead ultra thin fine pitch dual flat no lead, package outline*. Small text changes.

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